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presented by Aram Sarkis Adourian

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Signature .....

Typed name Robert M. Westervelt, Chair

Signature .....

Typed name Michael Tinkham

Signature .....

Typed name Efthimios Kaxiras

Date September 6, 1996

Single Electron Transport in Parallel Coupled Quantum Dot Nanostructures

A thesis presented

by

Aram Sarkis Adourian

to

the Department of Physics

in partial fulfillment of the requirements

for the degree of

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in the subject of

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For my parents

ABSTRACT

This thesis presents an experimental study of low-temperature electron transport in parallel coupled double quantum dot systems. The devices are fabricated in GaAs/AlGaAs heterostructure material grown by molecular beam epitaxy and are patterned using electron-beam lithography. The quantum dots are defined in the two-dimensional electron gas in the heterostructure using independently adjustable electrostatic surface gates. The gate geometry allows control over both the interdot tunnel barrier and the potential barriers which confine the electrons to each quantum dot.

The device dimensions are sufficiently small that dramatic effects due to capacitive charging of the coupled dot system by a single electron can be observed in the conductance characteristics at dilution refrigerator temperatures. The experiments are designed to probe explicitly the role of quantum mechanical interdot coupling in the double dot device. As the tunnel-coupling between the two dots is increased, the effects of quantum charge fluctuations in the system are observed in the low-temperature conductance data. The emergence of a set of secondary peaks in the conductance data resulting from interdot charge fluctuations is explored, and data is presented on the evolution of these peaks with temperature and interdot conductance.

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Acknowledgments

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CHAPTER I

Introduction

In the past few decades the demand for faster and more powerful computing systems has been the driving force behind the tremendous achievements in semiconductor device miniaturization. Most of the energy and resources in this effort have been devoted to scaling down device sizes and increasing component density in conventional CMOS VLSI (complementary metal-oxide semiconductor very large-scale integration) architectures. These efforts have pushed state of the art commercial electronic devices to sizes approaching 0.15 μm (as of this writing) and device densities of tens of millions per square centimeter. As these device sizes approach atomic scales, the quantum mechanical and discrete charge properties of individual electrons become important and may even come to dominate the transport behavior. An understanding of the basic physics of electron behavior in small structures is crucial to the success of further miniaturization of existing computing architectures, and may even point the way to new paradigms of computing.

One candidate for continuing this trend of device miniaturization and ushering in an approach to computing architectures is the field of "single-electronics" [Averin and Likharev, 1992]. Experimental investigation into this nascent field has been made possible largely by recent advances in nanolithography. These advances have allowed the fabrication of novel semiconductor devices in which electrons are strongly confined to small conducting regions within the crystal. In these devices, generally referred to as "quantum dots", striking phenomena can be observed at low temperatures due to the capacitive charging of the electron regions by a *single* electron. Such devices are also known as "single electron transistors", so called because the conductance through the

device can be modulated by the voltage on a capacitively coupled gate electrode. Indeed, the prospect exists for coding bits of information by the presence or absence of a *single* electron, promising extremely high scale integration and reduced power dissipation compared to current device technologies. Theoretical work has gone into designing practical devices such as logic gates and memory elements [Likharev, 1987; Tucker, 1992]. Novel approaches to computing which take advantage of the full quantum-mechanical nature in parameters such as charge, energy, and electron spin in quantum dots have also recently been developed [Bate, 1988; Lloyd, 1993; Bock, 1993]. In contrast with existing technologies, all of these effects in quantum dots improve, rather than degrade, with shrinking device size.

This thesis is motivated by the possibility of studying a system in which *two* quantum dots are fabricated in sufficiently close proximity that there is significant interaction with each other. Such coupled double quantum dot devices represent perhaps the first level of integration of individual quantum dots, in which the two elements interact with each other without interconnects. From the viewpoint of fundamental physics, the coupled dot system is interesting because the system can be adjusted from a regime in which the coupling is largely capacitive to one in which there is also an actual exchange of particles by quantum mechanical tunneling between the individual quantum dots.

The majority of this thesis describes the design, fabrication and measurement of a parallel coupled quantum dot device. Chapter II of this thesis reviews the sample fabrication techniques and the experimental methods used in acquiring the results presented in the subsequent chapters. Included in Chapter II is a review of the semiconductor heterostructure material in which the quantum dots are realized. We also discuss in detail the electron beam lithography process used to define the sub-micron size electrostatic surface gates which define the device geometry. The last section of Chapter II presents the cryogenic and low-noise electronics techniques required to observe the single electron

effects in our coupled quantum dot devices.

Chapter III presents a theoretical overview of the physics of coupled quantum dot devices. We begin by discussing the theory of the elements which constitute the parallel dot system, including the properties of quantum point contacts and individual quantum dots. We then summarize the results of recently developed theoretical models which offer insights and predictions about the behavior of a coupled quantum dot system in which both capacitive effects and interdot quantum charge fluctuations are included.

In Chapter IV we present the experimental results of low temperature conductance measurements performed on parallel coupled quantum dot devices. The experiments are designed specifically to probe the nature of the quantum mechanical interdot interaction. We compare our experimental results to the many-body theory presented in Chapter III and observe that the models which incorporate interdot charge fluctuations provide both a qualitative and quantitative understanding of the data.

Chapter V presents work which is a departure from the parallel quantum dot systems discussed in the previous chapters of this thesis. This work involves the development and fabrication of a novel integrated circuit which is designed to probe the high-frequency properties of individual mesoscopic devices. The device consists of an on-chip Josephson junction oscillator capacitively coupled to a quantum dot, eliminating the need for external sources of high-frequency radiation. The chapter outlines the development of the fabrication techniques which involve five separate sub-micron aligned patterning and processing steps required to construct a completed device. Experimental data from high-quality on-chip Josephson junctions is presented, and future directions for this work are proposed.

Finally, we summarize the results of this thesis and suggest future directions for building upon this work.

CHAPTER II

Sample Fabrication and Experimental Methods

2.1 Introduction

The first part of this chapter outlines the design and fabrication of coupled quantum dot devices. We begin by describing the GaAs/AlGaAs heterostructure material from which the samples are made and proceed to describe the device lithography and fabrication processes. The second part of this chapter describes the experimental apparatus used to make the measurements which are presented in this thesis.

2.2 GaAs/AlGaAs Heterostructures

The first step in achieving the electron confinement necessary for the fabrication of the quantum dots studied in this thesis is the formation of a two-dimensional electron gas (2DEG) inside a semiconductor wafer. High electron mobility semiconductor wafers consist of modulation-doped GaAs/AlGaAs heterostructures grown by molecular beam epitaxy (MBE), in which the 2DEG is physically separated from the ionized dopants by a spacer layer. MBE techniques are essential in achieving single-crystal films with atomically precise interfaces required for high quality semiconductor heterostructures. The GaAs/AlGaAs heterostructure material used in this work was grown by Ken Campman in the laboratory of Professor Art Gossard at the University of California at Santa Barbara. The MBE process is reviewed in Gossard [1982] and Herman and Sitter [1989], and

details specific to the MBE chambers at U.C. Santa Barbara may be found in Hopkins [1990] and Rimberg [1992].

A schematic cross section of the GaAs/AlGaAs heterostructure used in this work is shown in Fig. 2.1. The substrate is a commercial 2" semi-insulating [100] crystal orientation GaAs wafer. The first step in the MBE growth process is the deposition on this substrate of 2000 Å of GaAs followed by a superlattice consisting of approximately 25 periods of AlGaAs (20 Å) and GaAs (20 Å). The purpose of this step is to establish an atomically smooth wafer surface. Following another 10,000 Å of GaAs, whose purpose is to further separate the electron gas from the substrate, the $Al_{0.3}Ga_{0.7}As$ layer which defines the position of the interface where the 2DEG will form is grown. The $Al_{0.3}Ga_{0.7}As$ layer is interrupted by a fractional monolayer of n-dopant Si atoms setback 300 Å from the 2DEG and 220 Å from the previous GaAs layer. The 220 Å of AlGaAs beneath the delta-doping Si layer serves to reduce scattering at the 2DEG by the ionized impurities of the doping layer, while the 300 Å of AlGaAs above the Si layer is required to compensate the surface states. The last MBE step is the deposition of 50 Å of GaAs, whose purpose is to prevent oxidation of the Al in the AlGaAs layer once the wafer is exposed to atmosphere.

After the Si donors are ionized they reach thermal equilibrium with states at the surface and at the 2DEG interface. Since the conduction band energy in the GaAs is 260 meV lower than in the $Al_{0.3}Ga_{0.7}As$, it is electrostatically favorable for electrons from the dopant Si layer to move to the GaAs/AlGaAs interface. The positively ionized layer of Si atoms left behind results in an electric field whose direction is perpendicular to the growth direction. This electric field bends the conduction band of the GaAs and the AlGaAs as shown in Fig. 2.1, and creates the triangular well at the heterojunction interface in which the electrons are trapped to form the 2DEG. Electrons are transferred into the well from the donor Si atoms until the Fermi level of the well matches the chemical potential of the donor layer. In addition to transferring charge into the 2DEG well, the Si dopant layer also

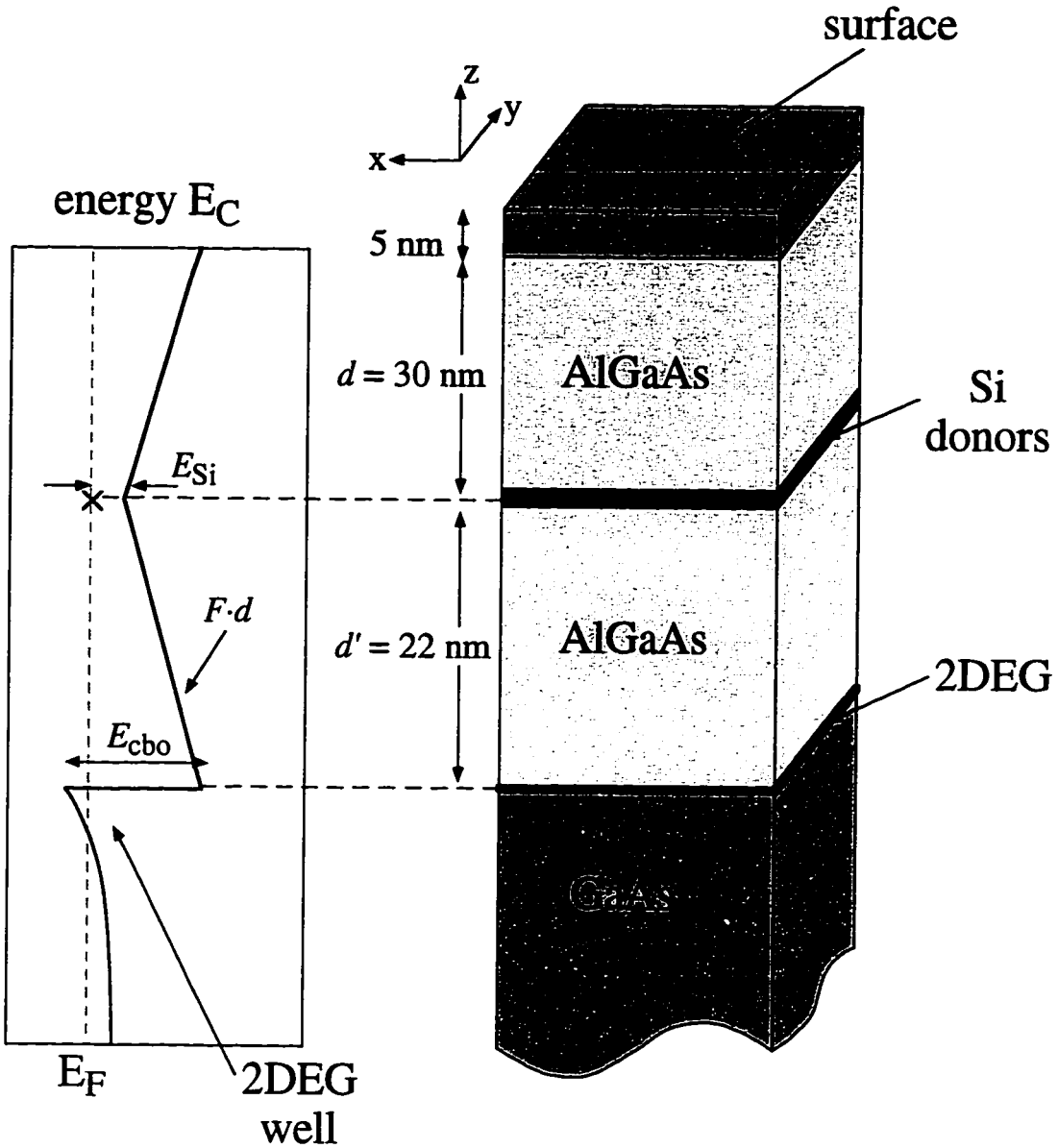


Fig. 2.1 Schematic cross-section of GaAs/AlGaAs heterostructure showing Si dopant layer and GaAs/AlGaAs interface where 2DEG forms. Also shown is the corresponding conduction band edge vs. distance from the surface. The 2DEG forms in the triangular well which results from both the interface conduction band discontinuity and the electrostatic potential of the donor layer.

supplies charge to satisfy the surface states which lie 800 meV below the conduction band edge.

Electrons in the 2DEG are free to move perpendicular to the growth direction and thus have a free particle energy spectrum $E = \hbar^2(k_x^2 + k_y^2)/2m^*$, where the electron effective mass in GaAs is $m^* = 0.067\, m_e$. Parallel to the growth direction, however, the electrons are confined to two-dimensional subbands formed inside the triangular well at the GaAs/AlGaAs interface. At low temperatures and under typical doping concentrations, only the lowest subband in the interface well is occupied, and the electrons consequently have no degree of freedom in the growth direction. It is in this respect that the electrons at the interface are referred to as two-dimensional. We can model the potential energy profile at the well by considering the electric field due to the unscreened positive ionized donors. Neglecting the Hartree exchange terms, the potential energy is a simple triangular well, as shown in Fig. 2.1:

$$V(z) = \begin{cases} +\infty & \text{for } z < 0 \\ Fz & \text{for } z \geq 0 \end{cases} \qquad (2.1)$$

where z = 0 is at the interface. The quantity

$$F = \frac{4\pi e^2 n_s}{\varepsilon} \cong \frac{1.81}{\varepsilon} \frac{\text{meV}}{(10^{11}\text{cm}^{-2})\,\text{Å}} \qquad (2.2)$$

represents the electric field due to the unscreened positive donors, n_s is the areal sheet density of electrons in the well, and $\varepsilon = 13$ is the dielectric constant of GaAs. Variational methods applied to the Schrodinger equation with this triangular potential profile yield Airy functions as approximate solutions to the Hamiltonian, with the approximate ground state energy given by

$$E_o \equiv \left(\frac{\hbar^2}{2m^*}\right)^{1/3}\left(\frac{9\pi e^2 n_s}{16\varepsilon}\right)^{2/3}. \qquad (2.3)$$

An estimate of the 2DEG areal sheet density can be obtained by analyzing the electrostatics of the conduction band through the heterostructure. Fig. 2.1 illustrates a simple model which shows the conduction band energy as a function of depth through the wafer. Equilibration between the Si donors and the 2DEG at low temperatures implies:

$$E_{Si} + Fd - E_{cbo} + E_o + E_F = 0 \qquad (2.4)$$

where $F \sim n_s$ as defined in equation (2.2), $E_o \sim n_s^{2/3}$ is defined in equation (2.3), $E_{Si} \approx$ 80 meV is the depth of the Si donor levels below the conduction band edge, $E_{cbo} \approx 260$ meV is the conduction band offset between AlGaAs and GaAs, $E_F = \pi\hbar^2 n_s/m^*$ is the Fermi energy, and d is the setback distance between the interface and the Si donors. In practice, the value of the setback distance d is the parameter which is controlled during MBE growth to determine the ultimate equilibrium sheet density in the 2DEG.

In addition to the carrier density of the 2DEG, MBE growth allows some degree of control over the electron gas mobility as well, albeit to a lesser extent. There are a variety of sources of scattering in the 2DEG which degrade the mobility of the electron gas. One intrinsic source of scattering over which the MBE grower has little control is contamination of the MBE chamber which results in the introduction of random impurities in the crystal. For example, despite the ultra-high vacuum techniques used in MBE growth, scattering from ionized contaminant carbon acceptors is believed to be a significant limiting factor for 2DEGs with mobilities in the range of $\mu = 10^6$ cm^2/Vs. One source of electron scattering which can be minimized by varying growth parameters is the random impurity potential at the interface due to the ionized Si donors. The undoped spacer layer which separates the Si

dopants from the interface is intended to physically separate the 2DEG from the positively charged donors and thereby reduce the electrostatic interaction which leads to elastic scattering in the 2DEG [Stormer *et al.*, 1981]. By making the setback between the dopants and the interface larger, effectively placing the 2DEG deeper in the wafer, the electrostatic influence of the ionized Si atoms becomes attenuated and resulting mobility in the 2DEG is enhanced. The tradeoff however is that the minimum feature size definable by electrostatic surface gates scales with the depth of the 2DEG, so that a shallow 2DEG is desirable for definition of mesoscopic devices. For the Coulomb blockade experiments described in this thesis, faithful reproduction of the electrostatic gate geometry at the level of the 2DEG was more important than high electron mobility, and consequently a relatively near surface electron gas wafer was used. Two wafers with similar growth profiles, labelled as KC3 and KC7, were used; their characteristics are given in Table 2.1.

wafer	d (Å)	d'(Å)	μ (cm^2/Vs)	n_s (10^{11} cm^{-2})
KC3	200	220	700,000	3.7
KC7	300	220	560,000	3.5

Table 2.1 Wafer characteristics for the material used in the experiments of this thesis. Mobility μ and areal sheet density n_s values were measured at U.C. Santa Barbara at 1.5 K unilluminated.

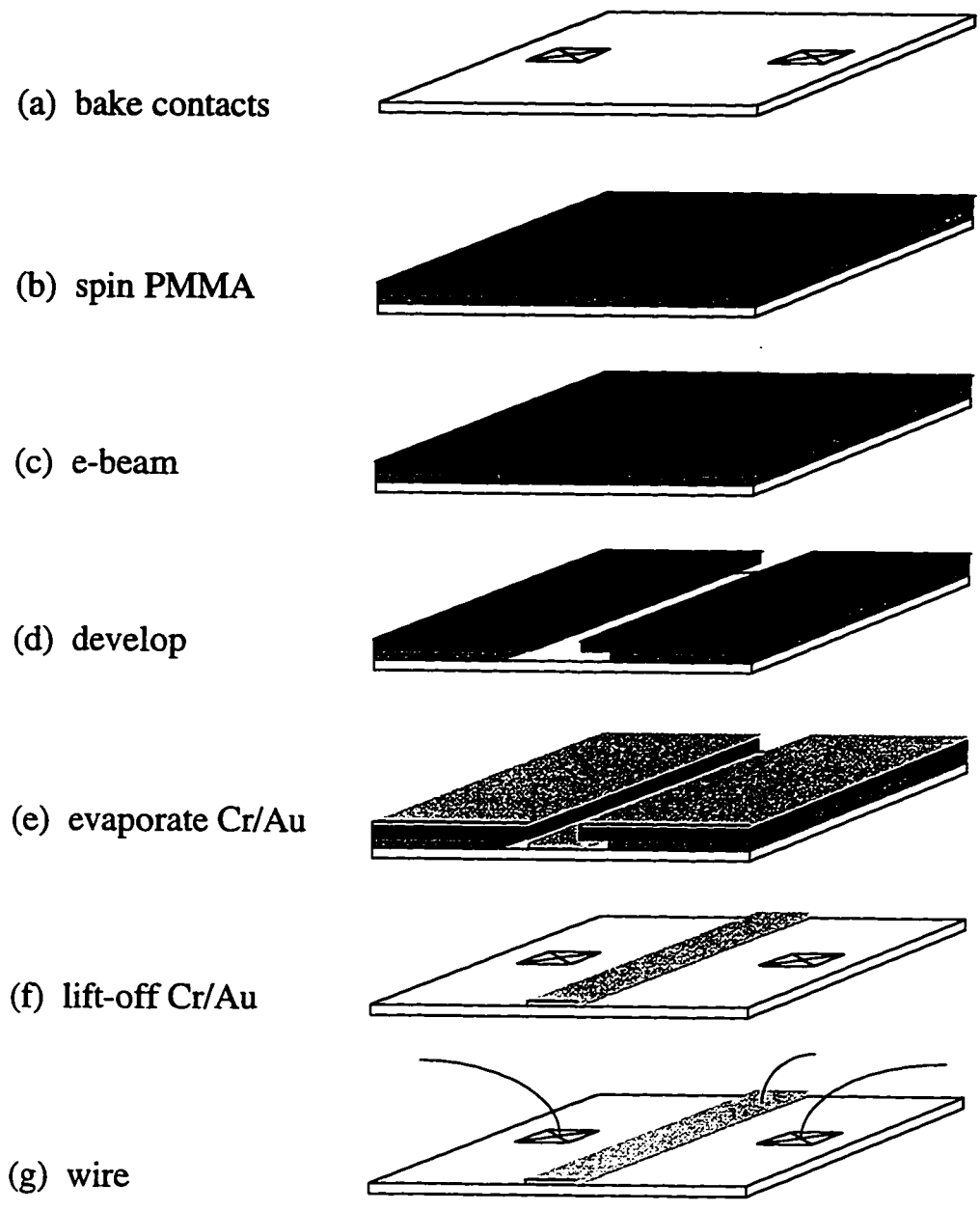


Fig. 2.2 Fabrication steps for split-gate defined semiconductor 2DEG devices described in text.

2.3 Device Fabrication

We will describe in the following sections the steps involved in processing the semiconductor heterostructure material to fabricate the devices which were used to obtain the results reported later in this thesis. Device fabrication consists of four main steps:

(*i*) ohmic contact formation

(*ii*) electron beam lithography patterning

(*iii*) gate metallization

(*iv*) wiring to gates and ohmic contacts

The following sections will outline the procedures involved in each of these processing steps.

2.3.1 Ohmic Contact Formation

As described in Sec. 2.2, the 2DEG in our semiconductor heterostructures is separated from the surface by a AlGaAs barrier which is typically several hundred angstroms thick. Many different techniques have been developed for making electrical contact to the buried 2DEG layer which are ohmic and robust at millikelvin temperatures and at high magnetic fields [Palmstrom and Morgan, 1985; Look, 1989]. For the devices described in this thesis, two different choices of material have been used as ohmic contacts to the 2DEG: (1) indium metal, and (2) Au/Ni/Ge alloy.

Indium Contacts

We will first describe the process which uses indium metal to form the contact to the 2DEG. The contacting process involves baking the indium into the semiconductor sample by which it alloys with the GaAs crystal via thermal diffusion and forms a graded $In_x(Ga:Al)_{1-x}As$ region [Woodall et al., 1981]. This process has been developed and improved upon by many of the past and current graduate students in the Westervelt group [Hopkins, 1990; Rimberg, 1992; Baskey, 1994; Waugh, 1994; Yang, 1995] and we present here a distillation of often empirically derived methods. The particular procedure, specifically the annealing recipe, has been optimized to yield reliable contacts for wafers KC3 and KC7 which were the wafers from which the devices studied in this thesis were fabricated.

1. Clean the sample chip thoroughly in boiling trichloroethylene (TCE) for 10 min to degrease the surface. After the beaker has cooled, place in ultrasound bath and ultrasound clean for an additional 10 min. Transfer sample to acetone and ultrasound for 10 min. Repeat with methanol. Leave sample in methanol until ready to apply indium metal.

2. Clean all tools which will be used in a similar manner. Tools which will be needed include teflon rollers and pads, and teflon-coated tweezers and metal tweezers.

3. Cut a small length (~1 cm) of 0.5 mm diameter In wire (Alpha Products, 99.999%) and place on cleaned teflon pad. Using a new sterile #11 scalpel blade, scrape the surface of the In wire to remove the native oxide layer and expose fresh metal. Be sure to wipe the blade clean (on filter paper) to remove dirty In from the blade after each scrape. This step and all steps through step 8 are conveniently done under a 1× to 4× magnifying scope.

4. Flatten the wire to a width of approximately 0.75 mm using teflon roller.

5. Cut the flattened wire piece to desired size (typically ~0.3 mm x 0.3 mm) without touching the scraped surface. Keep in mind that the final contact area will be ~30% larger than the initial piece of In.

6. Using scalpel or a pair of tweezers, transfer the In piece on the chip in the desired location so that the scraped In surface meets the wafer surface. The In should stick well to the clean chip surface.

7. Using clean teflon-coated tweezers, press firmly down on the In to ensure good physical contact. This will further increase the footprint of the contact.

8. Repeat steps 5 to 7 for each remaining contact, rescraping the In wire surface for each.

9. Place the sample on the nichrome tape heater in the Lucite oven [described in Hopkins, 1990]. After sealing the chamber, flush oven with forming gas (20% H_2:80% He) for 5 min with the silver ball on the flowmeter centered at a value of '3'. Forming gas prevents oxidation of the Indium and GaAs at high temperatures as hydrogen is a reducing agent.

10. Increase voltage to heater until thermocouple reads 105 °C. Maintain at 105 °C for 5 min to drive off water and solvents from the chip. Note that the thermocouple on the strip heater is type "K".

11. Hold at 180 °C for 5 min to fully melt indium (T_{melt} = 157 °C) and wet surface with metal.

12. Ramp up to 400 °C (should take approximately 20 sec to reach 400 °C) and bake at 400 °C for 60 sec. Monitor thermocouple temperature and adjust as necessary to maintain at 400 °C.

13. Reduce heat to 180 °C and anneal for an additional 5 min.

14. Turn heater off and let oven cool to room temperature maintaining forming gas flow.

After the annealing process, the sample is mounted on a chip carrier with carbon paint in order to test the contacts. Clean gold wires are attached to the In contacts by pressing into the metal with tweezers. The other ends of the gold wires are attached to the appropriate contact pads on the chip carrier by: 1) lightly scraping the Au chip carrier contact pad with a clean scalpel blade, 2) placing clean indium metal on the chip carrier pads following a procedure similar to steps 3 through 7 above, and 3) pressing the free ends of the gold wires into the indium metal on the chip carrier contact pads. The sample chip carrier is then fitted into the contact testing dunker apparatus and inserted into a dewar of liquid He. Contacts are tested at 4.2 K by applying a dc current bias of 1 μA using a Lake Shore 110 or 120 fixed current source (Lake Shore Cryogenics, Westerville OH) and measuring the sample voltage with a Keithley 177 voltmeter (Keithley Instruments, Cleveland OH). Both the resistance and diodicity, measured by reversing the current polarity, is recorded for each pair of contacts. Diodicity is indicated when a different voltage is produced across the sample due to a change in the polarity of the bias current. Good quality contacts typically exhibit resistances of a few hundred ohms, and diodicities less than 5%. After testing the contacts, the chip is removed from the chip carrier and cleaned ultrasonically in TCE, acetone, and methanol to remove any contaminants from the wafer surface before lithographic processing.

AuNiGe Contacts

A recently developed alternate method of contacting the electrons in the 2DEG layer involves evaporating and annealing a thin film AuNiGe alloy instead of indium into the semiconductor heterostructure. While fabricating contacts using this choice of material necessitates a separate lithography step, it has resulted in increased yield (approaching

100%), lower contact resistance (typically a few tens of ohms), and more precisely defined contact areas. The electron beam lithography technique used for defining the contact areas is identical to that which will be described in the next section. Here, we outline the AuNiGe deposition and annealing procedure used for successfully producing contacts of typical areas 200 x 200 μm^2.

1. After completing electron beam lithography, develop PMMA and spritz sample thoroughly with isopropanol to quench the developer and remove developed PMMA residue. Dry thoroughly with ultra-high purity (UHP) dry N_2.

2. Immerse sample for no more than 5 sec in a diluted solution of ammonium hydroxide (5 parts distilled water:1part 30% ammonium hydroxide solution, by volume) in order to remove any surface oxide layer on the wafer. Immediately blow dry with UHP N_2. This step should be done just before loading sample into evaporator.

3. Mount sample chip(s) on the thermal evaporator stage which is dedicated for AuNiGe contact evaporations. Charge the Ni, Au, and Ge boats and evacuate the thermal evaporator chamber to high 10^{-7} Torr range.

4. Evaporate in sequence: 50 Å Ni, 50 Å Au, 250 Å Ge, 400 Å Au, 100 Å Ni, and 200 Å Au. It is important that the sample stage be air-cooled using the compressed air feedthrough into the evaporator since excessive heating of the stage during evaporation may damage the PMMA resist layer.

5. Immerse sample in acetone for at least several hours to liftoff redundant PMMA and metal. After all redundant metal has lifted off, spritz the chip thoroughly with acetone followed by methanol. Inspect the sample with a microscope to ensure there are no unwanted areas of remaining AuNiGe metal, as any such regions may form unintentional contacts to the 2DEG. Any such areas which have not lifted off can usually be removed by re-immersing chip in acetone and treating with ultrasound for a few minutes.

6. Place the sample on the nichrome tape heater in the Lucite oven [described in Hopkins, 1990]. After sealing the chamber, flush oven with forming gas (20% H_2:80% He) for 5 min with the silver ball on the flowmeter centered at a value of '3'.

7. Increase voltage to heater until thermocouple reads 105 °C. Maintain at 105 °C for 5 min to drive off water and solvents from the chip. Note that the thermocouple on the strip heater is type "K".

8. Hold at 250 °C for 10 sec (start timing when temperature reads 210 °C)

9. Ramp up to 410 °C (should take approximately 20 sec to reach 410 °C) and bake at 410° C for 15 sec. Monitor thermocouple temperature and adjust as necessary to maintain at 410 °C.

10. Turn heater off and let oven cool to room temperature maintaining forming gas flow.

After annealing, mount the sample on a chip carrier as described in previous section. In contrast to indium contacts the AuNiGe thin film contacts may be wirebonded to the contact pads on the chip carrier. At 4.2 K, contact resistances should be typically a few tens of ohms, with diodicity < 5%. After completion of contact testing, the sample should be removed from the chip carrier and thoroughly cleaned ultrasonically in TCE, acetone, and methanol.

2.3.2 Gate Design and Electron Beam Lithography

Gate Design

The most versatile way to achieve electron confinement in the remaining two dimensions, i.e. in the plane of the 2DEG, is by the split-gate method schematically illustrated in Fig. (3.1). A sufficiently negative voltage, V_d, applied to a metallic surface gate results in depletion of electrons directly underneath the gate. As the gate voltage is made more negative, electrons in the channel formed by the two halves of the split-gate are depleted by the fringing fields of the gates, but at a slower rate. Davies [1988] has derived an expression for the ratio of the depletion voltage V_d, and the voltage V_p at which the channel formed by the split gates is pinched off:

$$\frac{V_p}{V_d} = \left(1 - \frac{2}{\pi}\arctan\frac{w}{2d}\right)^{-1} \qquad (2.5)$$

where w is the lithographic width of the gap between the split-gates and d is the depth of the 2DEG below the surface. It is important to choose a reasonable value of w/d so that a V_d is not so large as to induce appreciable gate to gas leakage. For typical doping levels, $V_d \sim -0.3$ V, so that a width-to-depth ratio $w/d \sim 4$ yields a reasonable pinchoff voltage of $V_p \sim -1.0$ V.

Electron Beam Lithography

Electron beam lithography is currently the most versatile and reliable technique of patterning surface split-gates for semiconductor devices with features smaller than 100 nm. A general overview of electron beam lithography and competing technologies is given in

[Newman, 1980]. Most research electron beam lithography systems, including the one at Harvard University, consist of a commercial scanning electron microscope which has been adapted for lithography purposes. In an electron beam system, electrons from a cathode filament are accelerated by a large voltage (typically tens of kV) and focused by magnetic lenses to form a narrow beam whose spot size is limited to a few nanometers by the electrostatic Coulomb repulsion of the electrons. The position of the electron beam spot on the sample is controlled by sets of very high precision magnetic deflection coils. The Harvard lithography system consists of a JEOL JSM-6400 scanning electron microscope (JEOL Ltd., Tokyo, Japan) which has been interfaced with a Hewlett-Packard Vectra 386/25 microcomputer. Special software, the Nanometer Pattern Generation System (NPGS) developed by J.C. Nabity Lithography Systems (Nabity Systems, Bozeman MT), permits the user to control the relevant parameters of the electron beam, such as beam position, beam current density, and exposure time. For lithography, the samples are coated with a thin (typically a few hundred angstroms) layer of polymethylmethacrylate (PMMA) resist, a cross-linked organic polymer (OCG Chemicals, West Patterson NJ). In such a resist system, the electron beam breaks the bonds which bind together the monomers in a resist molecule, and renders the molecules soluble in a chemical developer. After development, the remaining PMMA acts as a positive resist mask for subsequent processing steps such as metallization or etching. The minimum feature sizes are generally limited to tens of nanometers, primarily by the backscattering of electrons into the resist layer from the GaAs surface [Parikh and Kyser, 1979; Wittels, 1980].

The resist used in fabricating the parallel quantum dot device described in this thesis is a bilayer consisting of a bottom layer of low molecular weight (496 K) PMMA and a top layer of heavier (950 K) PMMA, as shown in Fig. 2.2(b). The bilayer serves to provide a natural undercut after development, as shown in Fig. 2.2(d), since the lower molecular weight PMMA is more sensitive to the electron beam and is exposed to a greater extent than

the top layer for a given beam dose. This undercut will facilitate liftoff of the redundant metal after metallization, as explained in the next section. The bilayer PMMA is applied to the sample chip using a commercial spinner (Headway Research, Garland, TX) located in class 100 facility in the Gordon McKay Laboratory clean room. It is crucial that the sample be free of debris during the PMMA application process lest any contamination settle on the chip surface during spinning. The procedure for applying the PMMA bilayer is outlined below; all steps are preformed in the inner class 100 clean room.

1. Rinse two new Pasteur pipettes (VWR Scientific, Boston MA) thoroughly with methanol and blow dry with filtered nitrogen gas. Preheat hotplate to 180 °C.

2. Carefully center sample chip on spinner chuck and set speed and spin time to desired values. In order to minimize particulate generation, avoid excessive movements and avoid placing head into fume hood.

3. Attach eyedropper bulb to one of the cleaned pipettes and fill with approximately 1 ml of 496 K PMMA solution (2% PMMA by weight). Place one drop on center of chip and spin at 4000 rpm for 60 sec.

4. Place chip on hotplate and bake at 180 °C for 20 min.

5. Remove sample from hotplate and let cool for about 1 min.

6. Center chip on spinner chuck and spin at 500 rpm while placing a drop of 950 K PMMA on sample using second pipette. As soon as the droplet of PMMA solution hits the sample, quickly switch to spin speed of 4000 rpm. The purpose of the initial 500 rpm spin is to prevent the chlorobenzene in the second drop from dissolving the previously applied layer.

7. Bake at 180 °C for 20 min.

This recipe results in a final PMMA bilayer thickness of approximately 1500 Å, which is

sufficiently thick to allow for easy deposition and liftoff of a few hundred angstroms of metal. A successful resist deposition results in uniform coverage of the sample surface area. If upon visual inspection of the chip surface a large number of interference fringes of different hues are seen, this likely indicates nonuniform resist coverage which may result in nonuniform lithography results over the chip area. If necessary, the PMMA can be stripped from the chip by immersing it in acetone and the process restarted.

The next step in the gate fabrication process as shown in Fig. 2.2(c) involves exposure of the pattern in the scanning electron microscope (SEM) located in the MRL microscopy facility in Gordon McKay Laboratory. The GaAs sample chip is mounted onto a cylindrical brass sample holder for insertion into the SEM. Since it is crucial to have the chip lie as flat as possible on the sample mount to minimize focusing errors during writing, especially for the smallest scale features, a special sample mounting system was developed. It consists of a custom made cylindrical brass sample holder with an internal channel which extends from the top to the side of the cylinder, a length of rubber hose, a plastic pipette attachment, and a suction bulb. The chip is placed over the hole at the top of the brass holder and the bulb is used to produce a temporary vacuum in the brass mount channel which draws the chip flat with the top surface. The sample can then be secured to the brass mount using two small droplets of conductive graphite paint (SPI, West Chester PA) on each side of the chip. The temporary vacuum prevents the graphite paint from being drawn under the sample due to capillary forces which would lead to an uneven sample surface. The bulb vacuum system can then be detached from the brass mount and the graphite paint left to dry under a 60 W incandescent bulb for 15 minutes. The graphite paint secures the sample to the brass mount and provides a conductive path to ground, preventing electrical charging of the sample surface during exposure to the electron beam. A few tiny specks of silver paint (SPI, West Chester PA) are then applied to the PMMA in a non-vital area on the sample surface to facilitate focusing and stigmation of the electron beam once the sample is

inserted in the SEM.

We now provide an overview of the procedures and techniques for successful patterning of submicron features using the SEM and the NPGS system. The drawing pattern is created using the commercially available computer-aided design software DesignCAD (American Small Business Machines, Inc., Pryor OK) with additional modules from the NPGS system. Within a single drawing, elements which are to be written at different magnifications or which are to receive different electron beam doses can be easily defined. A particularly helpful relation is that between the magnification setting of the SEM and the corresponding field of view of the electron beam, which provides an upper limit on the size of the features which may be written at a given magnification:

(Magnification) × (Field of view in μm) = 86,000 μm.

The order in which features are drawn in a pattern is also important: adjacent elements, two halves of a quantum point contact, for instance, should always be written consecutively to avoid errors due to beam drift or hysteresis. Sections of the drawing which are to be written at different magnifications should also overlap slightly, typically by a few microns; this is important since the SEM introduces origin offsets when switched between different magnification decades or condenser lens settings. These origin offset shifts seem to be filament-specific; they can be measured beforehand by writing a test pattern at the different magnifications and condenser lens setting to be used and measuring the origin offsets introduced by the SEM. The offsets measured in this manner can then be compensated for in the "MRF" file.

Once the design is complete, the "MRF" program takes the DesignCAD output and, with SEM beam currents and desired areal dosages inputted by the operator, creates a "PG" file containing the proper writing parameters. The parameters determine both the exposure

time of each point, which is controlled on the SEM via a TTL signal from the microcomputer which sets the external beam blanking shutter, and the position of the electron beam, which is controlled by a pair of 16-bit digital-to-analog converters interfaced with the magnetic deflection coils in the SEM. After the drawing pattern and the associated MRF are completed, the PG file can be tested by temporarily transferring the BNC cables (which originate at the microcomputer) from the SEM to a storage scope. In this way, the pattern writing can be verified on the storage scope before actual exposure of the sample.

Before loading the sample into the SEM it is important to ensure that the liquid N_2 trap of the chamber diffusion pump is full, in order to minimize the amount of backstreamed diffusion pump oil in the sample chamber. After loading the sample in the SEM, the accelerating voltage is turned on and the filament is saturated. An accelerating voltage of 35 kV was used to pattern all of the devices in this thesis, as this setting provides the smallest feature sizes. Lower accelerating voltages provide poorer lithography resolution, since low energy electrons are backscattered nearer to the surface of the GaAs and thus result in unwanted lateral overexposure of the PMMA. The beam parameters (saturation point, tilt, shift, stigmation, focus) are then optimized by focusing on a speck of silver paint away from any vital areas of the chip; this area of the PMMA will be unavoidably exposed during this optimization process. If the pattern to be written contains very fine elements (less than 1 μm), it is advisable to allow the filament to stabilize by waiting for approximately one hour before optimizing the beam parameters. The condenser lens setting, which determines the beam current, will depend on the magnification used and the spatial extent of the pattern to be written. Large areas written at lower magnifications generally require larger beam currents, corresponding to lower condenser lens settings. Typically, a pattern will contain different elements written at different condenser lens settings, and optimization of the beam parameters should be preformed at the highest condenser lens to be used in order to minimize drift in the beam current.

After the electron beam lithography has been completed, the exposed PMMA is developed and removed by immersing the chip, which has been taken off the brass sample holder, in a 3:1 volume mixture of isopropyl alcohol and methyl -isobutyl ketone with a small amount (1.3% by weight) of methyl ethyl ketone. The sample is left in the developer for 60 sec, and then vigorously rinsed in a strong stream of isopropyl alcohol and blown dry with ultra high purity dry N_2. Viewing the developed sample under an optical microscope will provide a diagnosis of the success of the lithography. The development is best done just prior to loading the sample into the thermal evaporator for metallization, in order to minimize contamination of the freshly exposed GaAs surface.

2.3.3 Surface Gate Metallization and Wiring

Gate Deposition

A suitable choice of gate material must meet a number of criteria which include: ease of deposition in uniform thin films, easy liftoff, good adhesion to GaAs, and resistance to oxidation and diffusion into the GaAs crystal. No single metallic material alone meets all these criteria, so we choose a double metallization layer consisting of an initial deposition of a thin layer of Cr followed by a layer of Au. Gold is resistant to oxidation, has robust liftoff properties, and also has proven to be a good material for the wiring which is performed in subsequent steps; chrome has been shown to adhere very well to GaAs and acts as a barrier to the diffusion of Au into the GaAs crystal.

Deposition of the Cr/Au bilayer is performed in the thermal evaporator equipped with a diffusion pump and liquid nitrogen cold trap, located in the Gordon McKay Laboratory

clean room. There are three electrical feedthroughs into the bell jar vacuum chamber which carry several hundred ac amperes of current that heat tungsten or molybdenum boats, in which the material to be evaporated is placed. The sample is mounted approximately 30 cm above the source boats on a stage which can be cooled during evaporation by circulating air or liquid nitrogen. A plate mounted on an armature controlled via a mechanical feedthrough is used to shutter the sample stage. A 5 MHz Ag crystal (Phelps Electronics Inc.), placed adjacent to the sample stage, is monitored by a Sloan 200 Thickness Monitor and is used to track the deposition rate and accumulated thickness during evaporation. It should be noted however that profilometry studies have shown that the actual deposited film is consistently 20 to 30% thicker than that indicated by the thickness monitor readout. All thickness values quoted in the remainder of this section refer to the nominal thickness as read by the crystal thickness monitor.

For surface gate evaporation, it is important to use the dedicated Cr and Au copper electrode arms which fasten on one end to the electrical feedthroughs in the chamber, and on the other end to the source boats. Exclusive use of this stage and the dedicated electrode arms minimizes the danger of contamination of the sample and evaporator. Similarly, use of the dedicated stage for Cr/Au evaporations is recommended. The sample is held onto the sample stage using a series of physical clips which should not be overtightened lest they scratch the PMMA on the sample chip. A 4 inch chrome covered rod (R.D. Mathis, Long Beach CA) on electrode #1 is used as the Cr source. The gold source boat is a flat-bottomed alumina covered boat (R.D. Mathis); the purpose of the alumina is to prevent alloying of the gold with the boat material. The gold boat is charged with small pieces of gold (99.999% pure) which have been cleaned in TCE, acetone, and methanol. Both the Cr rod and the Au boat are positioned as close to each other as possible to eliminate shadow effects [Yang, 1995].

The chamber should be pumped down for at least a few hours until base pressure of

2×10^{-7} Torr is reached. The liquid N_2 trap on the diffusion pump lasts for approximately three to four hours, and should not be allowed to run dry. Before deposition onto the actual sample, which should be protected by the closed shutter when not exposed to the evaporation sources, both the Cr rod and the Au should be pre-heated and cleaned for 100 Å each. For single layer metallic surface gates, it was found that a 100 Å of Cr followed by 250 Å of Au provided sufficient adhesion to the GaAs and produced easy liftoff. If subsequent wiring is to be done using the wirebonder instead of manually, a thicker (500 Å) layer of Au should be deposited. Typical deposition rates are 1 to 2 Å/sec for Cr and 3 to 5 Å/sec for Au. The significant amount of power dissipated in the bell jar during evaporation in addition to the heat transferred to the sample stage by the hot metal atoms can heat the sample and cause a hardening and cracking of the PMMA layer leading to liftoff difficulties. To prevent this, the sample stage is air-cooled throughout the evaporation process by attaching a compressed air supply hose to the stage cooling tube feedthrough and opening the wall air supply valve.

After the evaporation is complete the samples are allowed to return to room temperature before the evaporator is vented to atmosphere. The sample chip is then immediately immersed in acetone for liftoff of the PMMA and redundant metal. The liftoff process generally takes a few hours for large scale (> 1 μm) features; for smaller feature sizes immersion in acetone overnight is usually required. In order to inspect the sample for liftoff success without drying it, the chip can be temporarily moved to an acetone filled petri dish which will fit under the objective of an optical microscope. For liftoff of stubborn material, agitation of the sample immersed in acetone using ultrasound may be attempted, although caution must be used as there is a danger of unintentionally delaminating metal film elsewhere on the sample. With samples for which liftoff seems hopeless, as a last resort the sample may be placed in a petri dish of acetone and, under an optical microscope, an attempt may be made to jar loose the stubborn material using a (grounded) scalpel, followed by further ultrasonic agitation. After liftoff, the sample is rinsed thoroughly in

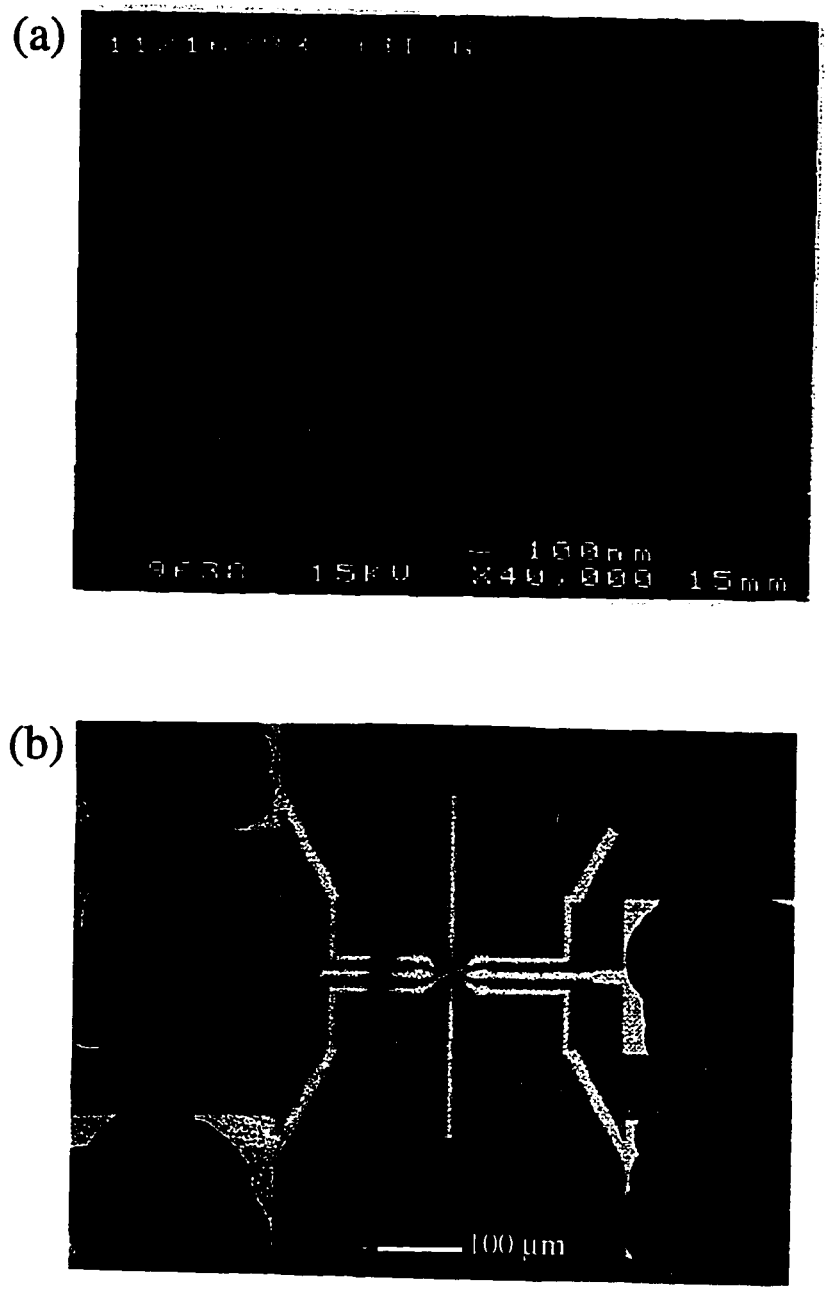


Fig. 2.3 (a) An example of successful electron beam lithography and gate metallization. Widths between gates are approximately 100 nm. (b) An expanded view of a sample which has been wired using indium metal. The indium pieces are the dark regions in the photograph. The wire connecting the two opposing gate pads on the top and bottom of the photograph is visible.

methanol and dried with a stream of dry filtered N_2 gas. At this point, all of the surface gates are electrically floating, and the sample must be handled very carefully to avoid destruction of the gates due to static discharge. Metal tweezers should exclusively be used, and when handling the chip the tweezers should not touch any of the thin film gates. Figures 2.3(a) and (b) illustrate successful electron beam patterning and gate metallization.

Wiring

After successful liftoff, the gates and ohmic contacts on the sample chip must be contacted electrically and connected in some manner to the measurement apparatus which is external to the cryogenic sample cooling system. The Westervelt group has adopted a modular sample mounting system which allows a sample to be easily interchanged between a variety of cryogenic and electrical measurement systems. The sample mounting scheme consists of a ceramic chip carrier (Jade Corporation, Southhampton PA), to which the sample chip is secured physically, and a socket, which is permanently attached to the cryogenic system and into which the chip carrier fits. Figure 2.5(b) includes a schematic of the chip carrier which is used in the Westervelt group. The chip carrier conforms to JEDEC A standards of the semiconductor industry, and consists of 28 external leads, each of which are connected to a wirebonding pad covered with 60 microinches of gold in the chip carrier interior. The sample chip is physically secured to the interior of the chip carrier with a small droplet of rubber cement, making sure to press down on the chip with a pair of grounded tweezers to ensure flatness.

Wiring the surface gates to the wirebonding pads on the interior of the chip carrier can be done either manually or using the Kulicke-Soffa 4123 wirebonder in the clean room. Here we will discuss general methods for manual wiring. Manual wiring entails cleaning

and placing small indium pieces onto the both the surface gates and the corresponding wirebond pads on the chip carrier, and connecting the two pieces of indium with a thin (1 to 3 mil) gold wire. The process for placing the indium on the sample and on the chip carrier is identical to that outlined in Sec. 2.3.1, steps 1 through 7. However, precautions must be taken to avoid destroying the surface electrodes by causing a static discharge across the micron-sized gaps between the gates. To prevent a build-up of static electricity on the chip surface, the sample mounted on the chip carrier is inserted into a 28-pin socket, all external pins of which have been soldered together and connected to earth ground. This socket is placed on a grounded aluminum sheet and handled only with grounded metal tweezers. The indium is applied by picking it up with a clean grounded scalpel and pressing it onto the surface gate with a pair of grounded tweezers. In a similar manner, indium is placed on the chip carrier bonding pads. Figure 2.3(b) illustrates successful indium wiring to surface gate pads of 200 x 300 μm^2. With adequate precautions, manual wiring of samples is a safe and effective process.

2.4 Cryogenics

Coulomb blockade effects and quantum confinement effects in single-electron systems are observable as long as the thermal energy of the electrons $k_B T_e$ is less than the relevant energy scale of the phenomenon being studied. For the experiments presented in Chapter 4, the Coulomb charging energy scale is $U \approx 300$ μeV and the single electron average level spacing is $\Delta E \approx 50$ μeV. To resolve these energies, experiments must be performed in a helium dilution refrigerator for which $T_e \approx 10$ μeV.

The dilution refrigerator system used to obtain the data in this thesis consists of a Kelvinox Model 100 dilution refrigerator insert and gas handling system from Oxford

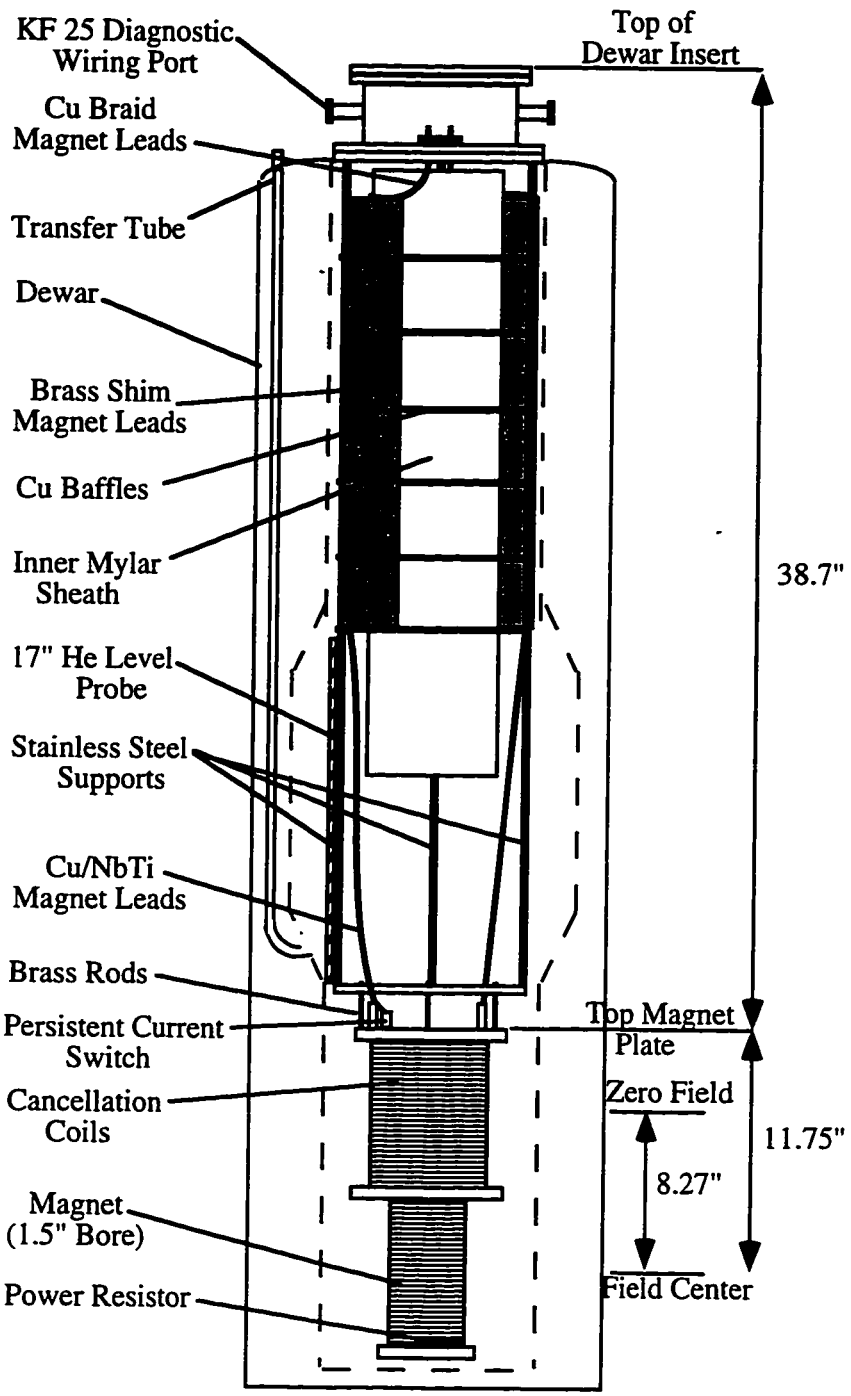


Fig. 2.4 Schematic view of of the dewar and magnet insert for the Kelvinox 100 system. The dilution unit itself slides inside the inner mylar sheath and mates to the top of the cryostat where it is bolted in place. Not shown are the concentric mylar sheaths that insulate the magnet leads from the baffles and dewar walls. After Katine (1996).

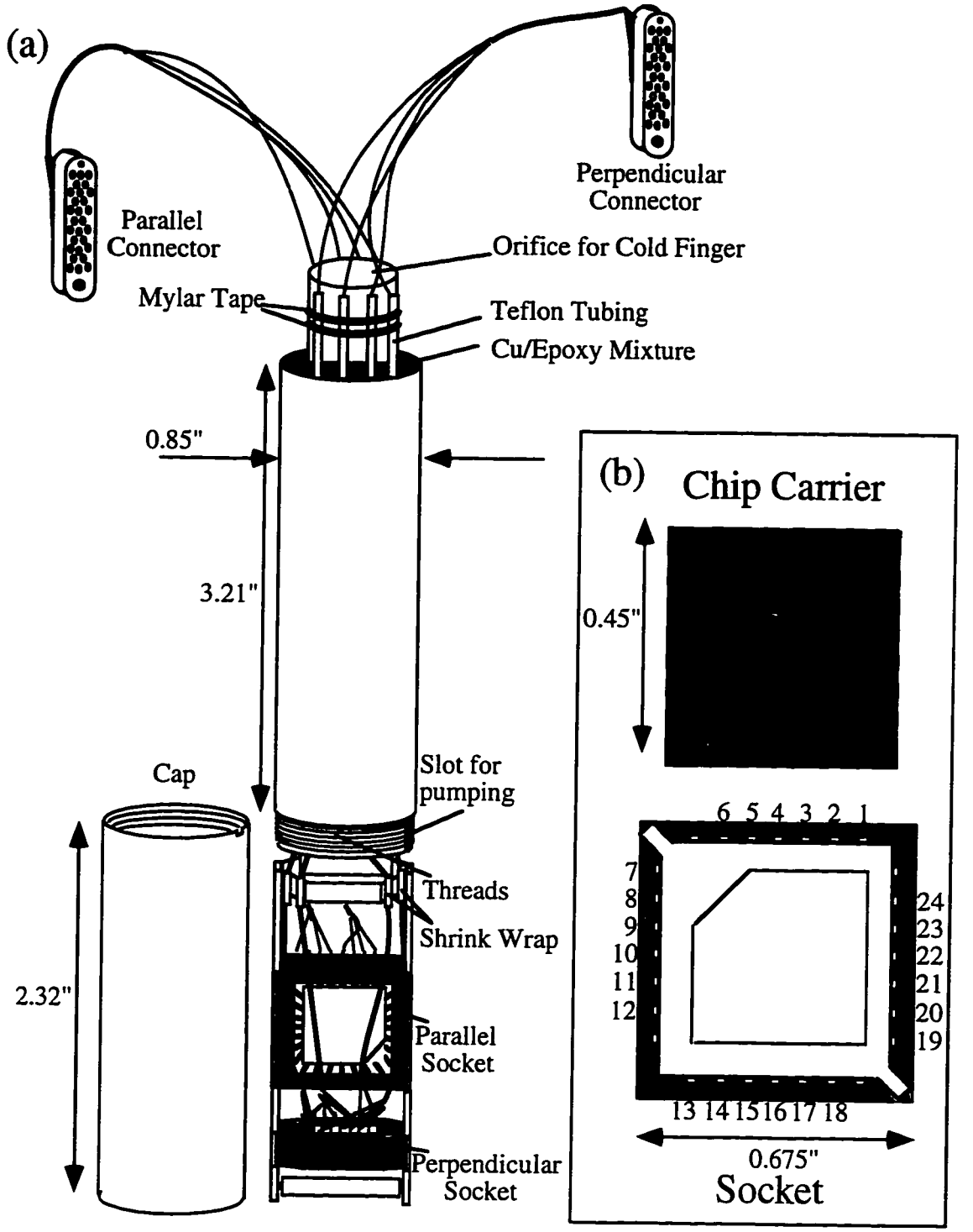


Fig. 2.5 (a) View of tailpiece assembly shown with radiation cap unscrewed. The tailpiece and cap are made of gold-plated stainless steel. (b) Schematic of chip carrier and socket. Leads are labeled corresponding to their pinouts on the Fischer connectors. After Katine (1996).

Instruments (Oxford Instruments, Witney, England) and a Precision Cryogenics cryostat (Precision Cryogenic Systems, Indianapolis IN) fitted with a 7 T superconducting magnet. A schematic diagram of the dilution refrigerator is shown in Fig. 2.4. To load and unload samples, the entire refrigerator insert is withdrawn from the cryostat, allowing easy access to the components internal to the inner vacuum chamber.

Principle of Operation

In this section we will briefly outline the principle of operation of a dilution refrigeration system. Detailed operating instruction for the Kelvinox Model are given in Appendix A and in the Kelvinox 100 Operator's Handbook from Oxford Instruments.

A mixture of two stable helium isotopes cooled below a critical temperature separates into two phases. The lighter "concentrated phase" is rich in ^{3}He while the heavier "dilute phase" consists mostly of ^{4}He. The concentration of ^{3}He in each phase is depends on the temperature of the mixture. Since the enthalpy of the ^{3}He in both phases is different, it is possible to "evaporatively cool" the mixture by evaporating the ^{3}He from the concentrated phase into the dilute phase.

The ^{4}He which constitutes the majority of the dilute phase is inert, and the ^{3}He moves through the liquid ^{4}He without interacting with the dilute phase medium. The cooling obtained by this process, which is analogous to evaporative cooling at a liquid-air interface, results in cooling of the mixing chamber and the sample. The process continues even at the lowest temperatures because the equilibrium concentration of ^{3}He in the dilute phase remains finite, even as the temperature approaches absolute zero.

The mixture is initially condensed from room temperature using the 1 K pot to cool the

mixture to 1.2 K. In order to establish the $^3He/^4He$ phase boundary, the mixture must be cooled below 0.86 K, the tri-critical point. This cooling comes from the still, which is the first part of the refrigerator to cool below 1.2 K. The incoming ^3He is further cooled by the still before it enters the heat exchangers and the mixing chamber. Gradually, the rest of the dilution unit is cooled until phase separation occurs.

To continuously cool the mixing chamber, the ^3He must be extracted from the dilute phase and returned to the concentrated phase, keeping the system in a dynamic equilibrium. To accomplish this, the ^3He is pumped away from the liquid surface in the still, which is typically at 0.6 K to 0.7 K. The vapor pressure of the ^3He is about 1000 greater than that of ^4He, so that the ^3He is pumped out of the still preferentially. The ^3He leaving the mixing chamber for the still is used to cool the returning flow of concentrated ^3He in a series of heat exchangers.

A sealed rotary pump external to the refrigerator is used to remove the ^3He from the still. The ^3He gas is then passed through filters and LN_2 and LHe cold traps to remove impurities and reintroduced into the refrigerator where it is cooled on the 1 K pot. A capillary tube flow impedance maintains a sufficiently high pressure in the 1 K pot for the ^3He gas to recondense.

The experimental sample apparatus is mounted on the mixing chamber, and consists of a socket system into which a chip carrier with a sample chip may be inserted. The design of this socket system is shown schematically in Fig. 2.5. Radiation shielding is a priority when considering the design of the sample leads from the socket to room temperature Fischer connector (Olson Associates, Boston MA) feedthroughs. The two paths by which radiation can reach the sample are (i) radiation transmitted down the electrical leads and (ii) ambient black-body radiation from warmer parts of the dilution refrigerator. To prevent radiation travelling down the leads, there are a series of copper-powder microwave filters heat-sunk to the 1 K pot and the mixing chamber through which all of the electrical leads

pass [Martinis, Devoret, and Clarke, 1987]. In addition, each electrical lead is interrupted by two 1 kΩ metal film blocking resistors, one of which is thermally anchored to the 1 K pot and the other to the mixing chamber. These resistors serve both to reflect the rf power due to 300 K blackbody radiation, and to protect the sample from voltage spikes by forming an RC filter in conjunction with the interlead capacitance (approximately 3 nF). For shielding the sample from ambient radiation inside the inner vacuum chamber, a cylindrical gold plated stainless steel cap is screwed onto the tailpiece over the sample, as shown in Fig. 2.5. Shielding of single-electron effect samples is discussed in detail elsewhere [Martinis, Devoret, and Clarke, 1987; Cleland, Schmidt and Clarke, 1992; Martinis and Nahum, 1993; Martinis, Nahum, and Jensen, 1994; Dresselhaus *et al.*, 1994].

2.5 Measurement Electronics

Figure 2.6 shows a schematic of the measurement circuit used to obtain the transport conductance data on the Coulomb blockade devices studied in this thesis. A small ac excitation voltage of 10 μV at 11 Hz is applied to the sample at one of the ohmic contacts to the 2DEG by voltage-dividing the output signal from the internal oscillator of an EG&G Princeton Applied Research (PAR) 124A lockin amplifier (Princeton Applied Research, Princeton NJ). The current which flows in the circuit as a result of this voltage bias is measured with a battery-powered Ithaco 1211 (Ithaco Inc., Ithaca NY) current preamplifier, whose output is read by the same PAR 124A. The lockin output is measured by a Fluke 8842A digital multimeter (Fluke, Everett WA) and sent to an Apple Macintosh microcomputer via an IEEE interface bus. The Macintosh acquires the data using routines

written in LabView (National Instruments, Austin TX) software, an instrumentation control program with a graphical interface [Mar, 1994].

One method of controlling the gate voltages on the sample involves full manual control over the fixed and ramped voltages. Figure 2.7 shows the circuit diagrams for the battery powered low-noise voltage circuitry used as the dc voltage sources in the experimental setup. The OP97 operational amplifiers used in these circuits were chosen specifically because of its low voltage noise, and they are powered by batteries to avoid ground loops. The output of these voltage sources is applied to the electrical lead feedthroughs on the dilution refrigerator via shielded twisted-pair BNC cables, interrupted at the top of the refrigerator by 60 Hz low-pass RC filters. The output of the ramped voltage source is read by a Fluke 8842A digital voltmeter and sent to the Macintosh computer. The LabView routine developed by Doug Mar [Mar, 1994] and updated by Carol Livermore logs the data from both the ramped voltage and the PAR 124 output. The main drawback of this method is that it requires typically tens of minutes to complete voltage sweeps of tens of millivolts, resulting in an increased probability that a charging event, such as those described in Sec. 4.3, will disrupt the data trace.

The second data acquisition system, designed and built by Carol Livermore, involves using the Apple Macintosh computer to control the ramped and some of the fixed gate voltages which are applied to the sample. The voltages are produced by 18-bit National Instruments digital-to-analog boards whose outputs are coupled to the sample through optical isolation amplifiers in order to avoid grounding problems. While a lockin amplifier is still used to read the current preamplifier output, the faster voltage ramp speed allows it to be operated at frequencies approaching 100 Hz. The main advantage of this semi-automated method is that it allows data to be taken at a much faster rate than the fully manual method, and allows the user to pre-program and cover a large range of parameter space with minimal intervention.

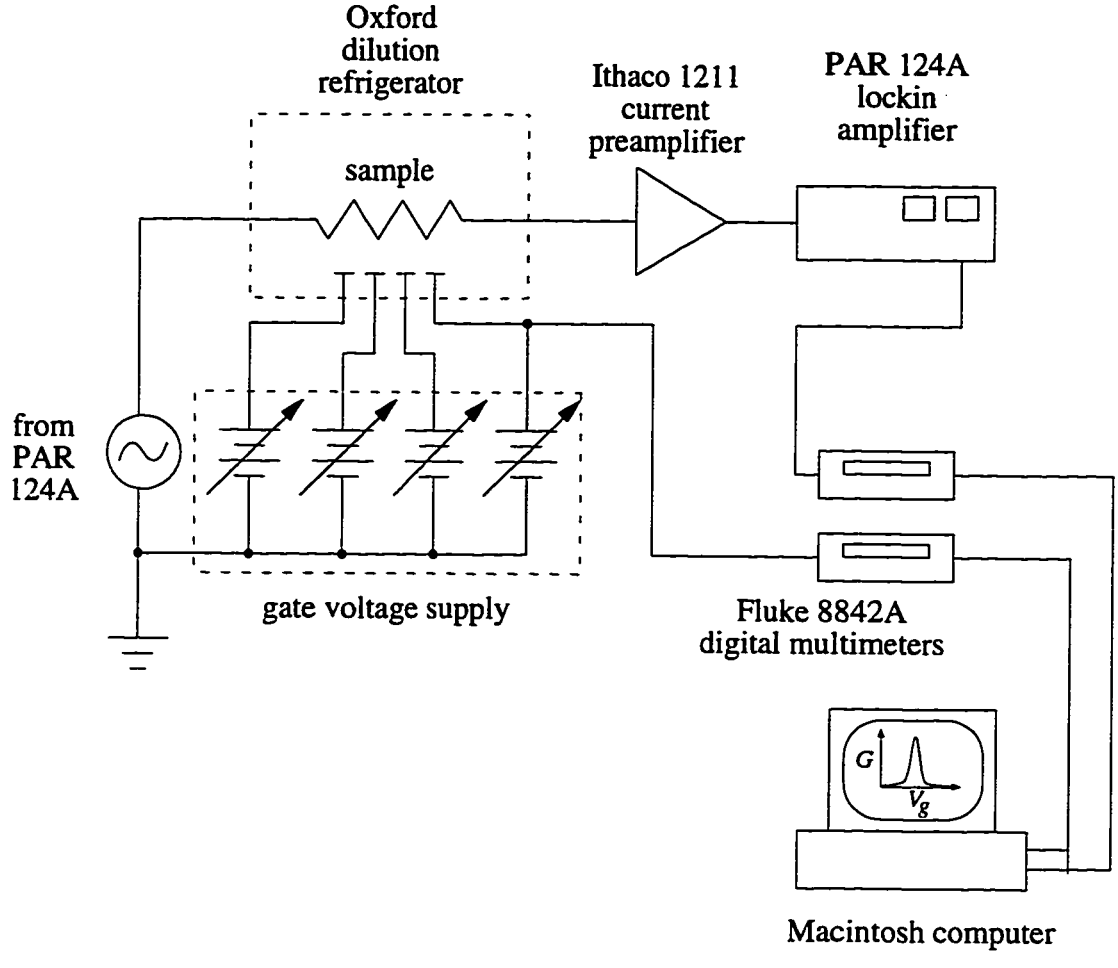


Fig. 2.6 Experimental set-up for Coulomb blockade experiments. The sample is voltage biased and the resulting current is amplified by current preamp and detected by lockin amplifier. The lockin output and ramped gate voltages are digitized by the Fluke 8842A multimeters and recorded on a Macintosh microcomputer running a LabView routine developed by Doug Mar and Carol Livermore.

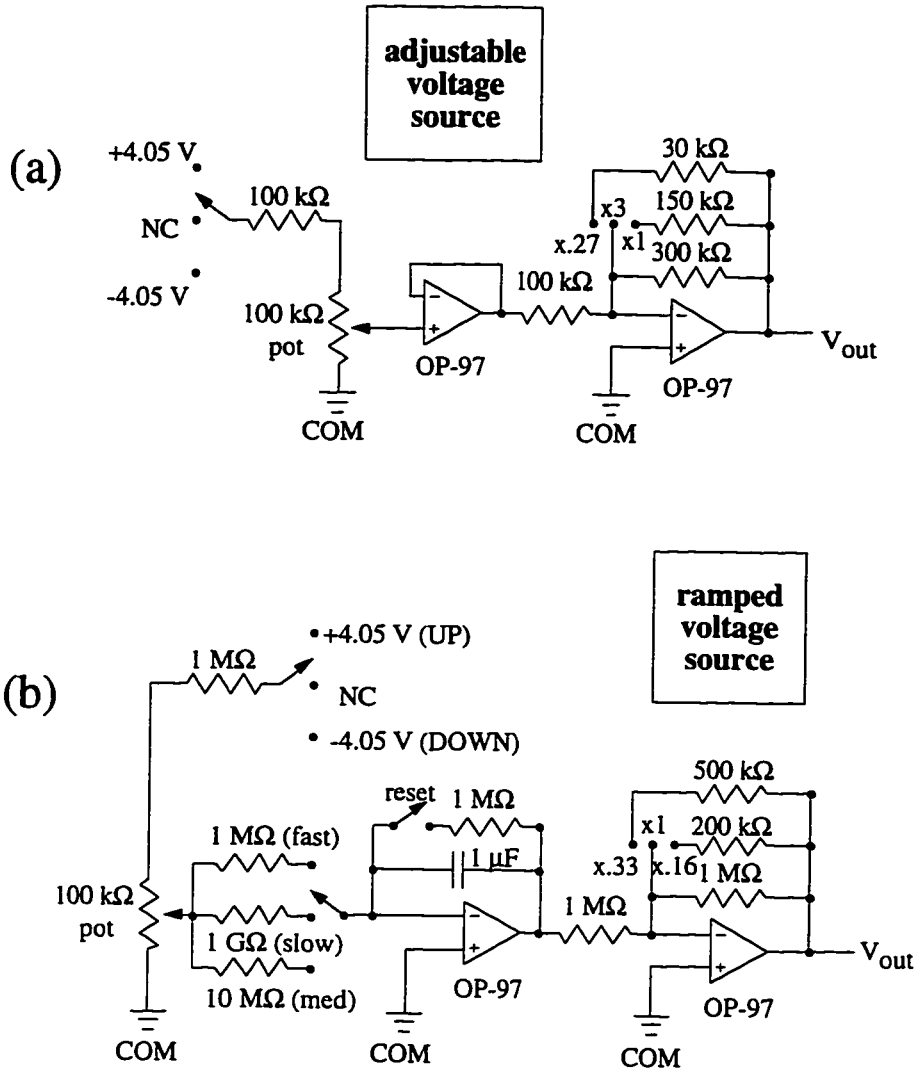


Fig. 2.7 Circuit diagrams for: (a) adjustable voltage source and (b) ramped voltage source. The voltage boxes have one ramped channel and seven adjustable voltage channels. All op-amps are powered by external 6V batteries.

CHAPTER III

Theory and Motivation

3.1 Introduction

Two-dimensional electron gas (2DEG) systems allow a remarkable degree of flexibility in device design and construction. In semiconductor 2DEG systems, metallic electrostatic surface gates can be used to laterally confine the electrons to regions that are effectively two, one, or zero dimensional, depending on the geometry of the gate pattern. Of course, the concept of dimensionality is dependent on the relevant length scales that characterize electron transport in the system, such as the mean free path l, the phase coherence length l_ϕ, and the Fermi wavelength λ_F.

The energy of a single electron in the absence of a magnetic field is given by

$$E(k_x,k_y)=\frac{\hbar^2\left(k_x^2+k_y^2\right)}{2m^*}, \tag{3.1}$$

where x and y are directions parallel to the interface and $m^* = 0.067m_e$ is the electron effective mass, which is isotropic in GaAs. From this expression, the number of electron states per unit area is calculated to be $n(E) = m^*E/\pi\hbar^2$, and the density of states is then:

$$\rho(E)=\frac{dn}{dE}=\frac{m^*}{\pi\hbar^2}, \tag{3.2}$$

taking into account the double spin degeneracy in the absence of a magnetic field. The

density of states is seen to be constant and independent of energy. As a consequence, the Fermi energy is simply proportional to the sheet density:

$$E_F = n_s/\rho \tag{3.3}$$

where n_s is the areal sheet density of electrons in the 2DEG. Typical sheet densities for the 2DEG material used in the experiments described in this thesis are $n_s \approx 3.6 \times 10^{11}$ cm^{-2}, implying a Fermi wavelength of:

$$\lambda_F = \sqrt{\frac{2\pi}{n_s}} \cong 40 \text{ nm} \tag{3.4}$$

3.2 Quantum Point Contacts

Shown in Fig. 3.1(a) is a schematic representation of the split gate method of confining the 2DEG to a narrow one-dimensional quantum point contact. The channel formed by this split gate method is considered to be one-dimensional in the sense that the width of the constriction is comparable to the Fermi wavelength λ_F. In this technique, the metallic gates are voltage biased sufficiently negative relative to the 2DEG that all the electrons underneath the gates are depleted. The voltage necessary for depletion can be estimated using the parallel-plate capacitor formula

$$\Delta n_s = \frac{\varepsilon \varepsilon_o}{ed} \Delta V_g \tag{3.5}$$

where $\varepsilon = 13$ is the dielectric constant of GaAs, d is the depth of the 2DEG from the

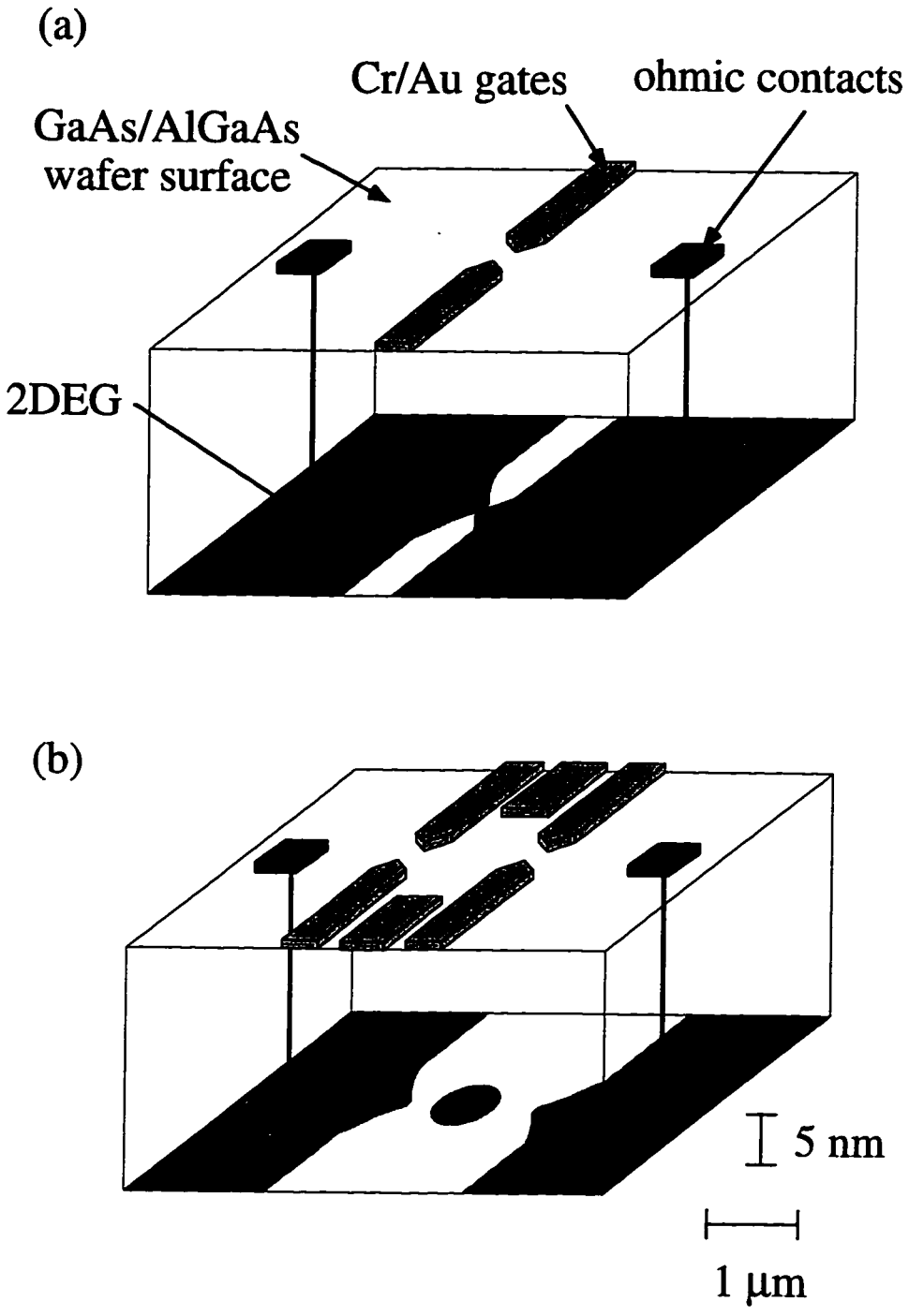


Fig. 3.1. Schematic picture of devices formed in GaAs/AlGaAs heterostructure 2DEG systems using split-gate method. A negative voltage applied to the Cr/Au surface gates depletes the electrons directly underneath. An increasingly negative gate voltage depletes electrons in the channel due to the fringing capacitance. (a) Quantum point contact formed in 2DEG with width 100 nm. (b) Isolated single quantum dot with diameter 500 nm. Scales are exaggerated for clarity.

surface of the wafer, and V_g is the gate voltage. For $\Delta n_s \approx 3.6 \times 10^{11}$ cm^{-2} and d ≈ 470 Å, typical parameters for the material used in this work, Eqn. (3.5) implies that a gate voltage of a few hundred millivolts is necessary to deplete the 2DEG, which is indeed what is seen experimentally. Upon further increase of the magnitude of the negative voltage on the gates, the width of the constriction in the 2DEG continuously decreases due to capacitive lateral depletion of electrons not directly underneath the gate, until the channel is pinched-off.

Shown in Fig. 3.2 is a typical conductance vs gate voltage trace for a quantum point contact at 4 K. The most striking feature of the data is the quantization of the conductance in units of $2e^2/h$, as first observed by van Wees *et al.* [1988]. The phenomena of conductance quantization can be understood by considering the transverse electric subbands which form in the one-dimensional constriction. We can treat the constriction of width w as an electron waveguide through which an integer number, $N = 2w/\lambda_F$, of transverse modes can propagate at the Fermi level, each mode carrying an equal amount of current. This equipartition rule results from the cancellation of the different electron group velocities at the Fermi level with the density of states in a two-dimensional system. Since the current through the quantum point contact is distributed evenly among the N modes in the constriction, the total conductance is the sum of the contributions of each mode [Landauer, 1957, 1988; Buttiker, 1986]:

$$G_{qpc} = \frac{2e^2}{h} \sum_{i=1}^{N} T_i \qquad (3.6)$$

where $0 \le T_i \le 1$ is the transmission probability of mode i. The factor of 2 in Eqn. 3.6 accounts for two spin states per mode in the absence of a magnetic field. For an ideal point contact, $T_i = 0$ for modes with energies above the Fermi energy, and $T_i = 1$ for modes below the Fermi energy. Deviations from such exact quantization are typically about 1%,

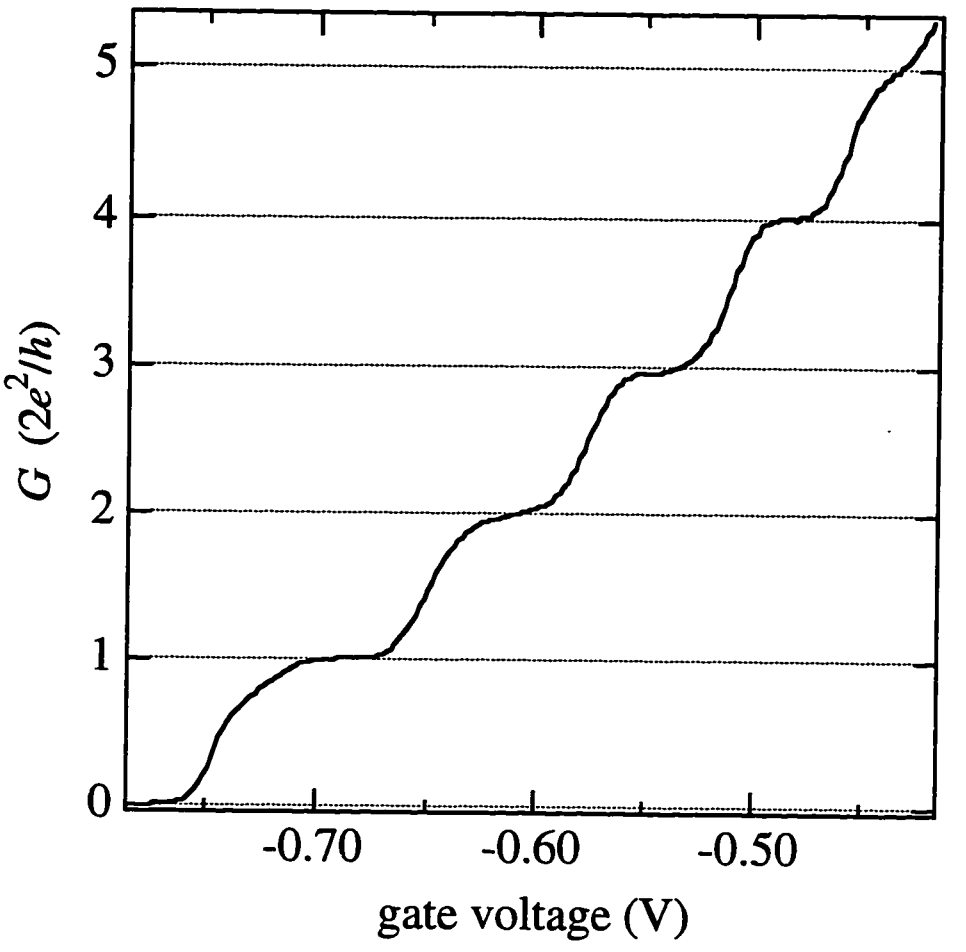


Fig. 3.2 Quantum point contact conductance G vs. gate voltage at 4 K showing the quantization of conductance in units of $2e^2/h$.

mostly due to the finite resistance of the wide 2DEG regions and quantum mechanical reflections from the non-adiabatic abrupt entrance and exit to the constriction.

More detailed theoretical analyses of quantum point contacts have been undertaken which involve solving the Schrodinger equation to match the electronic wavefunctions inside and outside the constriction [Szafer and Stone, 1989; Haanappel and van der Marel, 1989] and to include the effects of disorder [Haanappel and van der Marel, 1989; Nixon, Davies and Baranger, 1991; Laughton *et al.*, 1991; Timp, 1992]. For quantum point contact channels longer than the Fermi wavelength, interference resonances between the entrance and exit of the constriction are predicted to appear on the conductance plateaus. Including disorder in the models, whose origin in experiments is the random potential of ionized donors in the heterostructure, leads to less sharp conductance plateaus.

3.3 Single Quantum Dots

By arranging the surface gate geometry as shown in Fig. 3.1(b), we can use two quantum point contacts in series, with two additional confinement gates, to form an isolated region of 2DEG, referred to as a quantum dot. This structure is zero-dimensional in the sense that the electrons are confined to the 2DEG island defined by the negatively biased gates.

Electronic transport through a quantum dot is regulated by single-electron charging effects, also referred to as Coulomb blockade effects. The systems in which single-electron charging has been observed include small metal granule films, scanning tunneling microscope studies of small metallic grains, and metallic islands isolated by tunnel junctions [van Bentum, Smokers, and van Kempen, 1988; Fulton and Dolan, 1987]. Scott-Thomas et al. [1989] observed single-electron charging effects on double-gated

silicon MOSFETs where the electron confinement was achieved both by surface gates and randomly positioned charge impurities in the channel. This section describes the theory of single-electron charging in split gate quantum dots, such as those investigated in this thesis [Kastner, 1992; van Houten, Beenaker, and Staring, 1992].

GaAs/AlGaAs semiconductor heterostructures offer a generally greater degree of flexibility in the investigation of Coulomb blockade phenomena than other electronic systems. The split gate quantum point contacts which control the entrance and exit of the quantum dot introduce the ability to continuously control the height of the potential tunnel barrier which confines the electrons to the island. The tunneling of an electron onto the quantum dot changes the electrostatic potential of the dot by the charging energy $e^2/2C$, where C is the total capacitance of the island. In order to have a well-defined number of electrons on the island, the quantum fluctuations in the dot occupation number must be much smaller than one. A lower bound for the resistance R of the barrier required to achieve this confinement can be deduced from the Heisenberg uncertainty principle. The typical time Δt to charge or discharge the quantum dot is given by the RC time associated with the quantum dot, so the Heisenberg relation implies $\Delta t\, \Delta E = (e^2/2C)RC > h$. To reduce the uncertainty in the energy below the charging energy, the resistance of the barrier R should be much larger than the resistance quantum $R >> R_Q = h/e^2$.

Consider an island of electrons with charge Q and at a potential $\phi(Q)$ capacitively coupled to several other conductors, as depicted in Fig. 3.3(a). As indicated, the other conductors represent gate electrodes or the leads from which electrons tunnel on to or off the island. The charge Q on the island is related to the voltages on the other conductors $\{V_i\}$ by the capacitances $\{C_i\}$:

$$Q = \sum_i C_i(\phi - V_i). \tag{3.7}$$

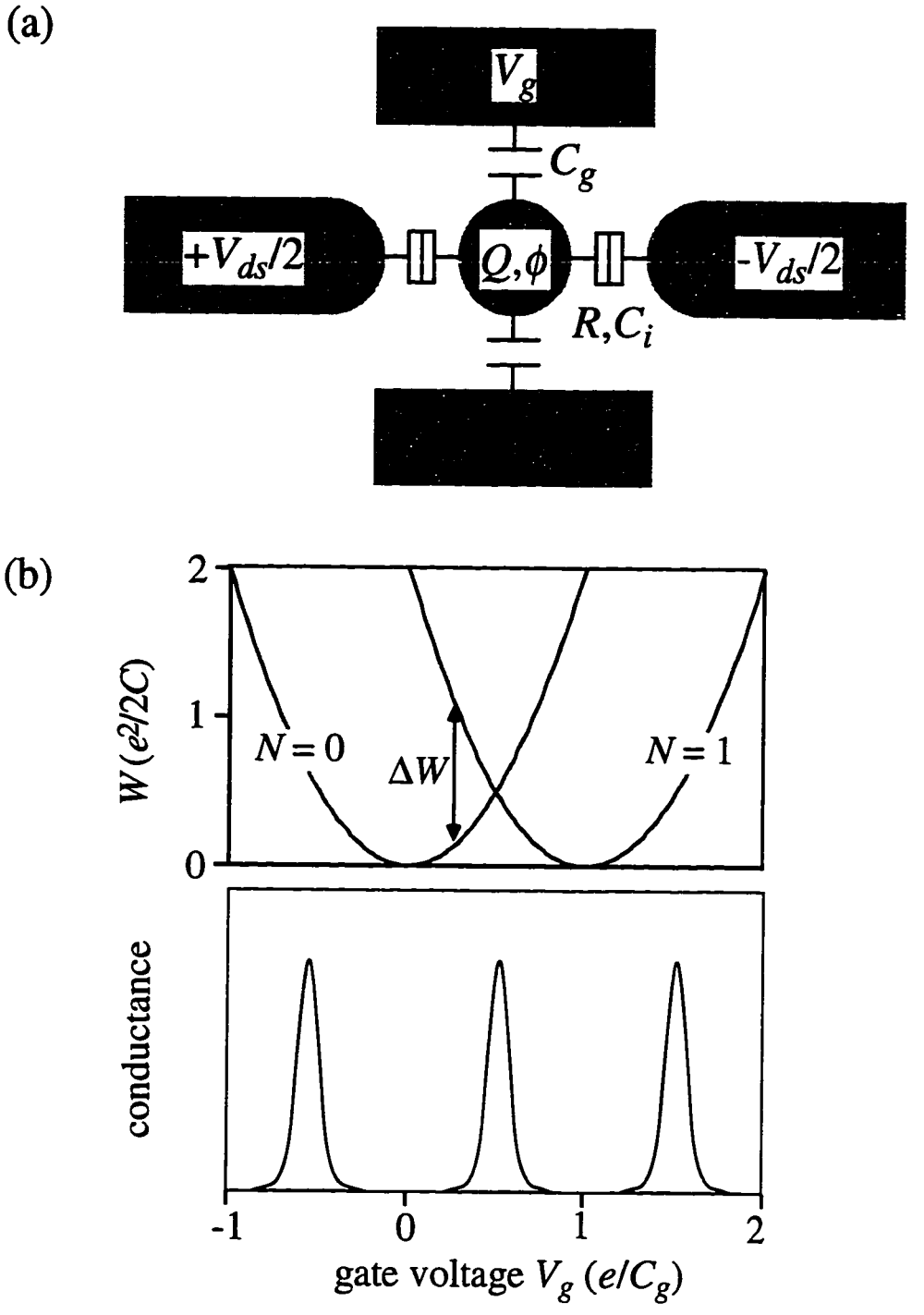


Fig. 3.3 (a) Schematic of capacitive charging model consisting of electron island with charge Q at potential ϕ capacitively coupled to other conductors, which may be leads or gates. Electrostatic energy W from Eqn. (3.11) for a single dot as a function of gate voltage V_g for $N = 0$ and $N = 1$ electrons on the island. The energy cost of ΔW adding an additional electron is also indicated. (c) Schematic single-dot conductance as a function of gate voltage V_g. Current flows when $W(N) = W(N + 1)$.

The electrostatic potential of the grain is then given by

$$\phi(Q) = \frac{Q}{C} + \frac{1}{C}\sum_i C_i V_i, \tag{3.8}$$

where $C = \sum_i C_i$. The electrostatic energy W required to bring a charge Q onto the island is

$$W(Q) = \int_0^Q \phi(Q')dQ' = \frac{Q^2}{2C} + \left(\sum_i \frac{C_i}{C} V_i\right) Q = \frac{(Q-Q_o)^2}{2C} - \frac{Q_o^2}{2C}, \tag{3.9}$$

where $Q_o = -\sum_i C_i V_i$. Since the island contains an integer number N of electrons, its charge is

$$Q = -Ne. \tag{3.10}$$

Up to a constant independent of N, Eqn. (3.9) becomes

$$W(N) = \frac{e^2}{2C}(N - N_o)^2 \tag{3.11}$$

where $N_o = -Q_o/e = \sum_i C_i V_i / e$.

Figure 3.3(b) illustrates the parabolic dependence of the system energy on the voltage V_g of one of the conductors capacitively coupled to the island, at different values of N and with the voltages on the other electrodes held constant. To minimize its electrostatic energy, the island must contain N electrons when $N - 1/2 < N_o < N + 1/2$ and $N + 1$ electrons when $N + 1/2 < N_o < N + 3/2$, which in Fig. 3.3(b) corresponds to N taking on the value corresponding to the lowest parabola. The energy cost of adding an additional electron to the island as a function of gate voltage V_g is given by:

$$\Delta W = W(N+1) - W(N) = \frac{e^2}{2C}\left(N + \frac{1}{2} - \frac{C_g V_g}{e}\right) \tag{3.12}$$

where C_g is the capacitance to the island of the electrode whose voltage is being varied. When the gate voltage is such that $\Delta W = 0$, then $W(N + 1) = W(N)$ so that the number of electrons can fluctuate freely between N and $N + 1$ and current can flow, one electron at a time, through the island. This degeneracy occurs when

$$V_g = \frac{e}{C_g}\left(N + \frac{1}{2} - \sum_{i \neq g} \frac{C_i V_i}{e}\right) \tag{3.13}$$

yielding a periodicity e/C_g in V_g. When V_g is not at one of these special degeneracy values, current flow through the island is impeded by the Coulomb blockade. This modulation of current through the quantum dot leads to conductance peaks as a function of gate voltage when the voltage on one of the electrodes is swept while keeping the other voltages fixed.

Quantum mechanical effects become important when the electron Fermi wavelength becomes comparable to the confinement length scale, and the classical orthodox mode presented above is no longer strictly valid. As a first approximation, the contribution of the quantized single particle energy levels to the system ground state energy $U(N)$ energy can be accounted for by adding the energy of the single particle states to the previously derived electrostatic energy of the island [Beenaker, 1991]:

$$U(N) = W(N) + \sum_{p=1}^{N} E_p = \frac{(Ne)^2}{2C} - Ne\sum_i \frac{C_i V_i}{C} + \sum_{p=1}^{N} E_p \tag{3.14}$$

where $\{E_p\}$ are the single particle energy levels measured from the bottom of the conduction band. This model neglects any many body effects other than the Coulomb

charging energy contribution. The energy cost of adding an additional electron to an island with N electrons now becomes

$$U(N+1)-U(N)=(N+\frac{1}{2})\frac{e^2}{C}-e\sum_i\frac{C_iV_i}{C}+E_{N+1} \qquad (3.15)$$

Taking into account the discrete energy levels leads to a spacing in gate voltage between successive current peaks of

$$\Delta V_g=\frac{e}{C_g}+\frac{C}{C_g}\frac{E_{N+1}-E_N}{e}=\frac{C}{eC_g}\left[(N+\frac{1}{2})\frac{e^2}{C}-e\sum_i\frac{C_iV_i}{C}+E_{N+1}\right]. \qquad (3.16)$$

The factor C/C_g represents the "lever arm" relating the changing gate voltage to the corresponding change of the bottom of the conduction band. For the experiments described in this thesis, $e/C_g \approx 7$ meV, while the energy level spacing $\Delta E \approx 50$ μeV, so that the the classical orthodox model remains a valid lowest-order approximation.

The description of Coulomb blockade phenomena above predicts the periodicity of the Coulomb oscillations as a function of gate voltage but is not sufficient to understand the amplitude and width of the conductance peaks. Detailed calculation of the conductance through a quantum dot was performed by Beenaker [Beenaker, 1991] using a rate-equation approach and Meir, Wingreen and Lee [Meir et al., 1991] using an Anderson model. Here, we will summarize the results of the rate-equation approach in the regime relevant to the experiments of Chapter 4. A thorough introduction to both methods is given by van Houten [Grabert, 1992].

The reservoirs, which are coupled to the quantum dot via tunnel barriers, are assumed to be large enough to be considered as a continuum of states whose occupancy at a temperature T is given by the Fermi-Dirac distribution

$$f(E)=\frac{1}{1+exp[E/k_BT]} \tag{3.17}$$

where all energies E are measured from the Fermi energy. The tunneling rate from the left (right) reservoir to the dot is denoted by $\Gamma_p{}^l$ ($\Gamma_p{}^r$), with the assumption that $k_BT >> h(\Gamma_p{}^l + \Gamma_p{}^r)$. The set of occupation numbers $\{n_p\}$, where $n_p = 1$ ($n_p = 0$) if level p is occupied (unoccupied), arranged according to a Gibbs distribution, characterizes the ground state of the quantum dot. The probability that the quantum dot is found in a particular state characterized by N and n_p is calculated by solving a kinetic equation.

The main result of Beenaker [1991] is that in the linear response regime the two-terminal conductance, defined as $G = I/V$ in the limit $V \to 0$, is given by

$$G=\frac{e^2}{k_BT}\sum_{p=1}^{\infty}\sum_{N=1}^{\infty}\frac{\Gamma_p^l\Gamma_p^r}{\Gamma_p^l+\Gamma_p^r}P_{eq}\left(N,n_p=1\right)\left[1-f\left(E_p+W(N)-W(N-1)-E_F\right)\right] \tag{3.18}$$

where $P_{eq}(N, n_p = 1)$ is the equilibrium probability that the quantum dot contains N electrons and that level p is occupied. The product of the distribution functions represents the probability that an electron in the reservoir has sufficient energy to tunnel into an unoccupied state on the island. If $k_BT << e^2/2C$, $P_{eq}(N, n_p = 1)$ will be weighted about one particular value of N.

Eqn. (3.18) reduces to simpler form in two limiting cases. In the limiting case of $k_BT << \Delta E << e^2/2C$ (ΔE is the energy level spacing) relevant to the experiments of Chapter 4, only a single electron state E_p on the dot is accessible, and Eqn. (3.18) reduces to

$$G=\frac{e^2}{4k_BT}\frac{\Gamma_p^l\Gamma_p^r}{\Gamma_p^l+\Gamma_p^r}\cosh^{-2}\left[\left(\frac{1}{2k_BT}\right)\left(E_p+\frac{e^2}{2C}\left(N+\frac{1}{2}-\frac{C_gV_g}{e}\right)\right)\right]. \tag{3.19}$$

The full-width at half-maximum of the conductance lineshape in this case is given by

$$\Delta V_{FWHM} \cong \frac{3.5k_BT}{e}\frac{C}{C_g} \tag{3.19b}$$

where C is the total dot capacitance and C_g is the capacitance of the dot to the gate being swept. In the classical limit of $\Delta E << k_BT << e^2/2C$, first investigated theoretically by Kulik and Shekhter [1975], Eqn. (3.18) becomes

$$G = G_{max}\cosh^{-2}\left[\left(\frac{1}{2.5k_BT}\right)\left(\frac{e^2}{2C}\left(N+\frac{1}{2}-\frac{C_gV_g}{e}\right)\right)\right] \tag{3.20}$$

$$G_{max} = \frac{e^2}{2\Delta E}\frac{\Gamma_p^l\Gamma_p^r}{\Gamma_p^l+\Gamma_p^r}. \tag{3.21}$$

As seen by the results in these two limiting cases, when the temperature is increased from $k_BT << \Delta E$ to $k_BT >> \Delta E$ the amplitudes of the Coulomb blockade oscillations evolve from a exhibiting a strong T^{-1} temperature dependence to being weakly temperature dependent. The conductance peak shape is similar in these two limiting cases, but the FWHM is approximately 1.25 times larger in the classical limit.

3.4 Coupled Quantum Dots

Less extensively studied than single-dot Coulomb blockade phenomena is the theory of electron transport through arrays of coupled quantum dots. Improving lithographic capabilities have recently made it possible to fabricate arrays of coupled quantum dots, defined electrostatically in semiconductor 2DEG systems, which allow a remarkable degree of control over both the interdot coupling and the coupling of the dots to the outside world.

The experiments described in Chapter 4 investigate the transport properties of such a system with two coupled quantum dots in the Coulomb blockade regime. Recent theoretical studies of such systems have yielded a variety of interesting new phenomena whose understanding necessitates going beyond the orthodox single-dot Coulomb blockade theory presented in the previous section.

3.4.1 Double Quantum Dots With Zero Interdot Tunneling

As a starting point, we will consider a system consisting of two quantum dots in which there is no exchange of electrons between the dots. Consequently, the number of electrons on each dot is an integer and is well-defined. The model used is illustrated in Fig. 3.4, showing the various capacitances and gate voltages involved. The total electrostatic energy $W(N_A, N_B)$ of this double-dot system with N_i electrons on dot i ($i = A,B$) is given by [Hofmann *et al.*, 1995]:

$$W(N_A, N_B) = \frac{1}{2} Q^T \begin{pmatrix} C_A & -C_{AB} \\ -C_{AB} & C_B \end{pmatrix}^{-1} Q \tag{3.22}$$

$$Q = \begin{pmatrix} eN_A - C_{1A}V_{g1} - C_{2A}V_{g2} \\ eN_B - C_{2B}V_{g2} - C_{1B}V_{g1} \end{pmatrix} \tag{3.23}$$

where the C_A and C_B represent the total capacitance of dot A and B respectively. Physically, this expression reflects the total electrostatic energy stored in the double-dot system as a result of the difference between the continuous polarization charge induced on the dots by the external gate voltage sources and the necessarily quantized charge residing

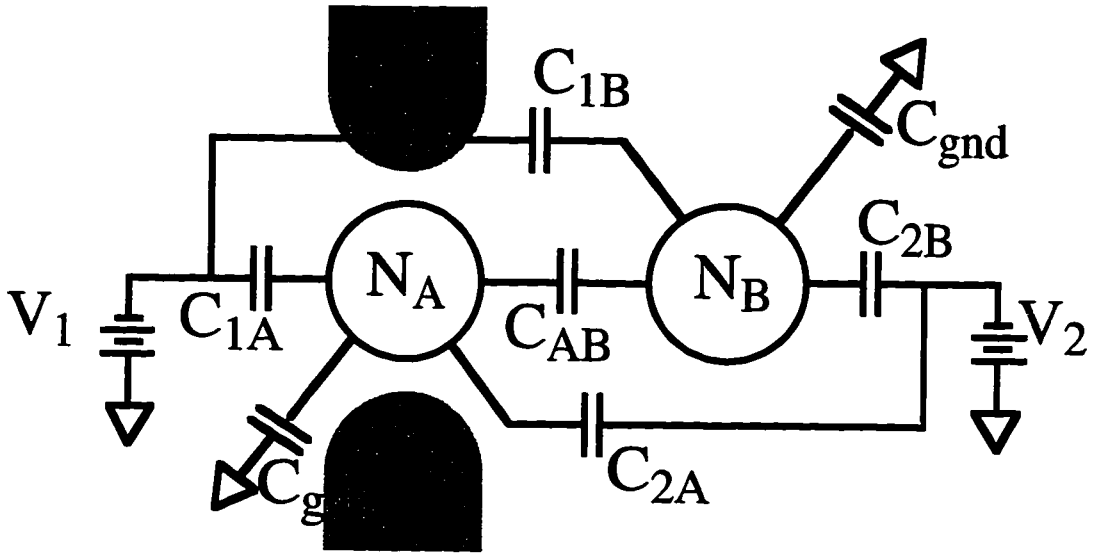


Fig. 3.4 Equivalent circuit of parallel coupled quantum dot system. Each dot i, i = A, B, has a capacitance C_{gi} to gate g and a capacitance C_{gnd} to ground. The darker areas represent the source and drain leads to dot A.

on each of the quantum dots. In the limit where the interdot capacitance C_{AB} and the cross capacitances of each gate are much smaller than all other capacitances (C_{1B}, C_{2A}, $C_{AB} \rightarrow 0$), Eqn. (3.22) reduces to

$$W(N_A, N_B) = \frac{(eN_A - C_{1A}V_{g1})^2}{2C_A} + \frac{(eN_B - C_{2B}V_{g2})^2}{2C_B} \tag{3.24}$$

which is simply the sum of the electrostatic energies of two separate non-interacting dots.

From Eqn. (3.22) we see that the energetically stable charge configuration of the coupled dot system in equilibrium is determined by the gate voltages V_{g1} and V_{g2} and the values of the partial capacitances C_{ij}.

Using Eqn. (3.22) and Eqn. (3.23) we can construct a "charging diagram", as a function of the two side gate voltages, which represents the stable charge configurations of the system. Such charging diagrams have been studied previously in the context of single quantum dots in high magnetic fields [Heinzel et al., 1994, Evans et al., 1993] and the electron pump [Pothier et al., 1992]. Several periods of the charging diagram for the double-dot system are plotted as a function of the gate voltages V_{g1} and V_{g2} in Fig. 3.5(a). The boundaries in this plot correspond to points of degeneracy in the total electrostatic energy of the coupled dot system where $W(N_A,N_B, V_{g1}, V_{g2}) = W(N_A \pm 1,N_B \pm 1, V_{g1}, V_{g2})$. As denoted in Fig. 3.5(a), each unit cell in the diagram corresponds to a different charge state of the double-dot system. The solid line boundaries denote a change in the total number of electrons ($N_1 + N_2$) in the system, while the dashed line boundaries correspond to internal redistribution of charge with no change in the total electron number. The precise shape of the unit cells depends on the particular values of the partial capacitances involved in the system. The voltage spacings Δ_i between various points in the charging diagram are analytic functions of the partial capacitances in the problem. In particular,

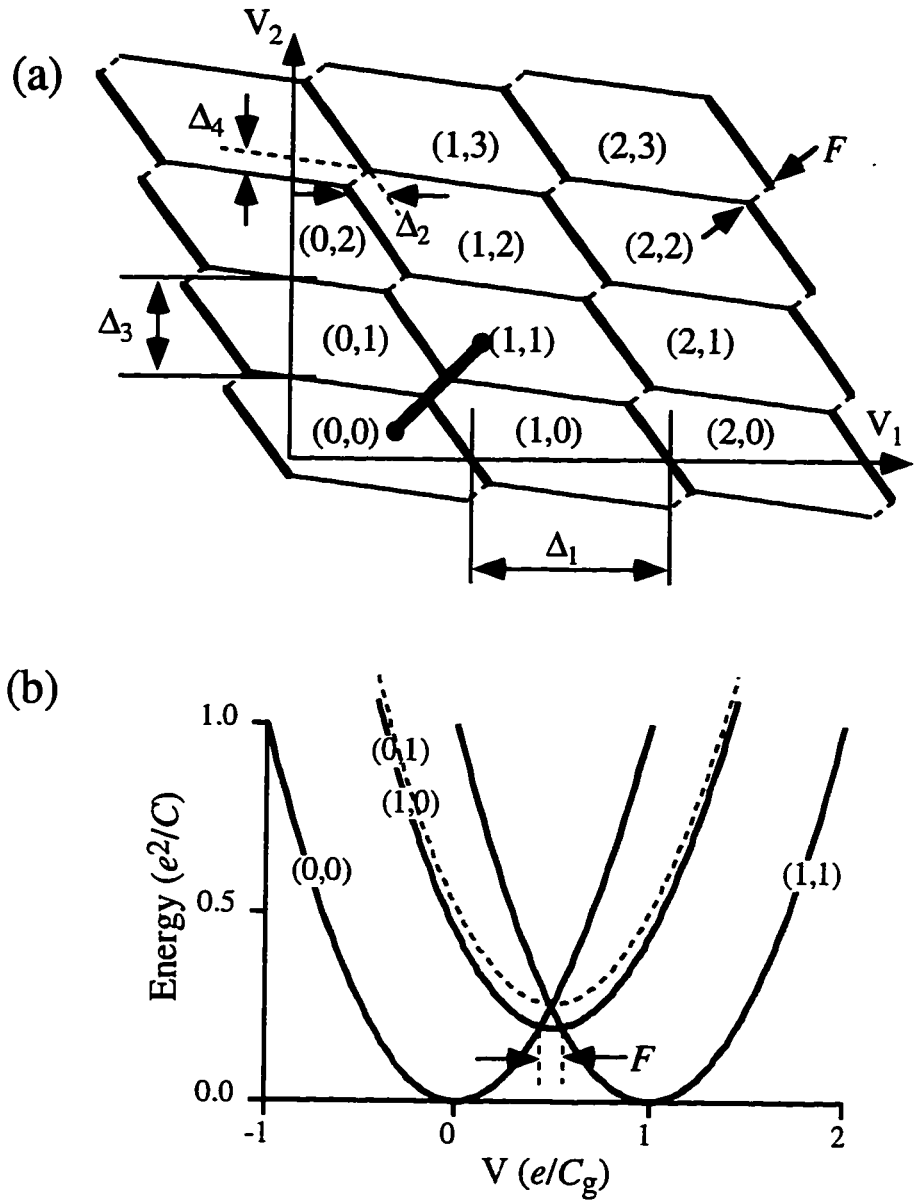


Fig. 3.5 (a) Charging diagram for coupled dot system. Each unit cell labelled by (N_A, N_B) corresponds to a different stable charge configuration with N_i electrons on dot i. The relation between the cell boundary separations (Δ_i) and the partial capacitances is discussed in the text. The splitting F between adjacent columns in the charging diagram arises from the finite interdot capacitance. (b) The electrostatic energy $W(N_A, N_B)$ along the dark line segment shown in (a).

$$C_{1A} = \left(\frac{e}{\Delta_1} - C_{1B} \frac{\Delta_2}{\Delta_1} \right) \tag{3.25}$$

$$C_{2B} = \left(\frac{e}{\Delta_3} - C_{2A} \frac{\Delta_4}{\Delta_3} \right) \tag{3.26}$$

$$C_{AB} = C_B \frac{\Delta_2}{\Delta_1}. \tag{3.27}$$

The structure in the charging diagram, tracing along the V_{g1} direction for example, represents single electron charging of dot A, similar to a single-dot experiment where one gate voltage is swept. The abrupt discontinuities between adjacent rows of unit cells occurs when the occupancy of the second dot, dot B, is changed by one electron, causing a discontinuous change in the electrostatic potential which influences dot A.

Some of the measurements reported in this thesis have been performed in a parallel dot structure in which the conductance is measured through one dot, as in Fig. 3.4. In such a device the linear conductance through one dot (dot A) is monitored as a function the voltages V_{g1} and V_{g2} on the two capacitively coupled side gates. The boundaries in the charging diagram which should be visible in such an experimental conductance sweep are those in which the total number $(N_1 + N_2)$ of electrons in the double-dot system changes by one. In particular, those boundaries which correspond to a change in the charge state of the main dot, dot A, are shown in bold in Fig. 3.5(a).

Shown in Fig. 3.5(b) is an illustration of the lowest electrostatic energy of the double-dot system as a function of the voltage along the segment highlighted in the charging diagram of Fig. 3.5(a). The total dot capacitances are assumed to be identical in this figure, $C_A = C_B \equiv C$. The dependence of each stable charge state, denoted by (N_A,N_B) where there are N_i electrons on dot i, on gate voltage is parabolic. The states with odd total

number, (01) and (10) in Fig. 3.5(b), are higher in energy than the states with even electron number, (11) and (00). Physically, this reflects the fact that in this model, an odd electron added to the system is constrained to occupy one dot or the other, introducing an excess electrostatic polarization energy into the system. The most energetically favorable charge configuration (N_A,N_B) corresponds to the lowest parabola at a given gate voltage. The splitting between adjacent columns satisfying (N_A,N_B) = constant, denoted by F in the charging diagram of Fig. 3.5(a) and in Fig. 3.5(b), is seen to arise from this excess polarization energy in the system. The dashed parabola in Fig. 3.5(b) represents the electrostatic energy of the odd electron state in the limit where the interdot capacitance C_{AB} and the cross gate capacitances vanish $(C_{1B}, C_{2A}, C_{AB} \rightarrow 0)$. It is seen that in the absence of an interdot capacitance, the excess electrostatic polarization energy attains its maximum value of $e^2/4C$ and the splitting F vanishes.

3.4.2 Double Quantum Dot With Finite Interdot Tunneling

The strictly capacitive model introduced in the previous section is inadequate to describe the electrostatics of a double-dot system in which there is finite interdot tunneling. When the interdot barrier is lowered sufficiently to allow electrons to tunnel between the two dots, the number of electrons on each dot is no longer well-defined. In this finite tunneling regime, a generally non-integer number of electrons on each dot will minimize the total electrostatic energy of the system. Calculations in this regime will predict the relative shifts in the ground state energies when tunneling is allowed between the dots. Physically, if electrons are shared between both dots in the system, any excess internal electrostatic polarization energy in the system will be relaxed, leading to a lowering of the ground state energy of the polarized charge configuration state. We seek to find a relation between the

interdot tunnel conductance, which characterizes the transfer of charge between dots, and the relative downward shift of the electrostatic energies of the polarized charge states. Several authors have independently undertaken a detailed theoretical treatment of electron transport through a double-dot system in the presence of finite interdot tunneling [Golden and Halperin, 1996; Matveev, Glazman, and Baranger, 1996]. The geometry studied consists of two identical quantum dots separated by an adjustable quantum point contact whose conductance is denoted by G_{int}. In this section we summarize their results.

Definition of the Model

The model double-dot Hamiltonian H used in the analysis explicitly includes a term, H_T, which describes tunneling of electrons through the barrier which separates the two dots. The Hamiltonian is given by $H = H_o + H_T$ [Golden and Halperin, 1996], where

$$H_o = K + V$$

$$K = \sum_{i=1}^{2} \sum_{\sigma} \sum_{k} \varepsilon_{ik\sigma} \hat{n}_{ik\sigma},$$

$$V = \frac{U}{2} \sum_{i=1}^{2} \left(\hat{n}_i - \frac{C_{gi} V_{gi}}{e} \right)^2,$$

$$H_T = \sum_{\sigma} \sum_{k_1 k_2} \left(t_{k_1 k_2} c^{+}_{2k_2\sigma} c^{+}_{1k_1\sigma} + \text{H.c.} \right) \tag{3.28}$$

and $i = 1,2$ is the dot index, σ is the index for the modes connecting the two dots through the internal quantum point contact, k is the index for all degrees of freedom not included in

the mode index σ, $\hat{n}_i$ is the number operator for dot i, $t_{k_1 k_2}$ is the tunneling matrix element between the wave function on dot 1 indexed by k_1 and the wavefunction of dot 2 (in the same mode) indexed by k_2, and $\varepsilon_{ik\sigma}$ is the kinetic energy of the single particle state on dot i indexed by k and σ.

Assuming an abrupt interdot tunnel barrier, which is justified because the length scale of the potential barrier induced by the internal quantum point contact is of the order of the Fermi wavelength, the interdot tunneling term H_T reduces to a form equivalent to that found in a tight-binding picture with two sites and intersite hopping. With this approximation for the interdot tunnel barrier, the double-dot model can be exactly mapped onto a problem considered by Glazman et al. [Glazman and Matveev, 1990] involving charge fluctuations of a single isolated dot connected to a large 2DEG reservoir by a single quantum point contact. The transformation to the one-dot model is analogous to a standard center-of-mass transformation from classical mechanics [Golden and Halperin, 1996; Matveev et al., 1996]. It yields the following form for the double-dot potential energy V, which is similar in form to that for a single-dot problem:

$$V = \frac{U}{4}\left(\hat{N}_{tot} - \Phi_{tot}\right)^2 + U(\hat{n} - \rho/2)^2 \qquad (3.29)$$

where $U = e^2/C$ is the the total charging energy of each individual dot, assumed to be identical for both dots, and $\Phi_{tot} = C_{g1}V_{g1}/e + C_{g2}V_{g2}/e$, $\hat{n} = (\hat{n}_1 - \hat{n}_2)/2$, and $\rho = C_{g2}V_{g2}/e - C_{g1}V_{g1}/e$ is the difference of the induced charges on the dots. In solving the model, it is more convenient to consider imbalances in the induced charge on each dot, represented by ρ, instead of the actual charge difference between the dots, $n = N_1 - N_2$. Solving this model single-dot Hamiltonian for the relative shifts of the $\rho = 0$ and $\rho = 1$ ground state energies will yield the downward shift Δ of the polarized charge state energy parabola illustrated in Fig. 3.6(b), and the consequent splitting F in gate voltage of the charge degeneracy points, shown in Figs. 3.6(a) and (b). More generally, since the

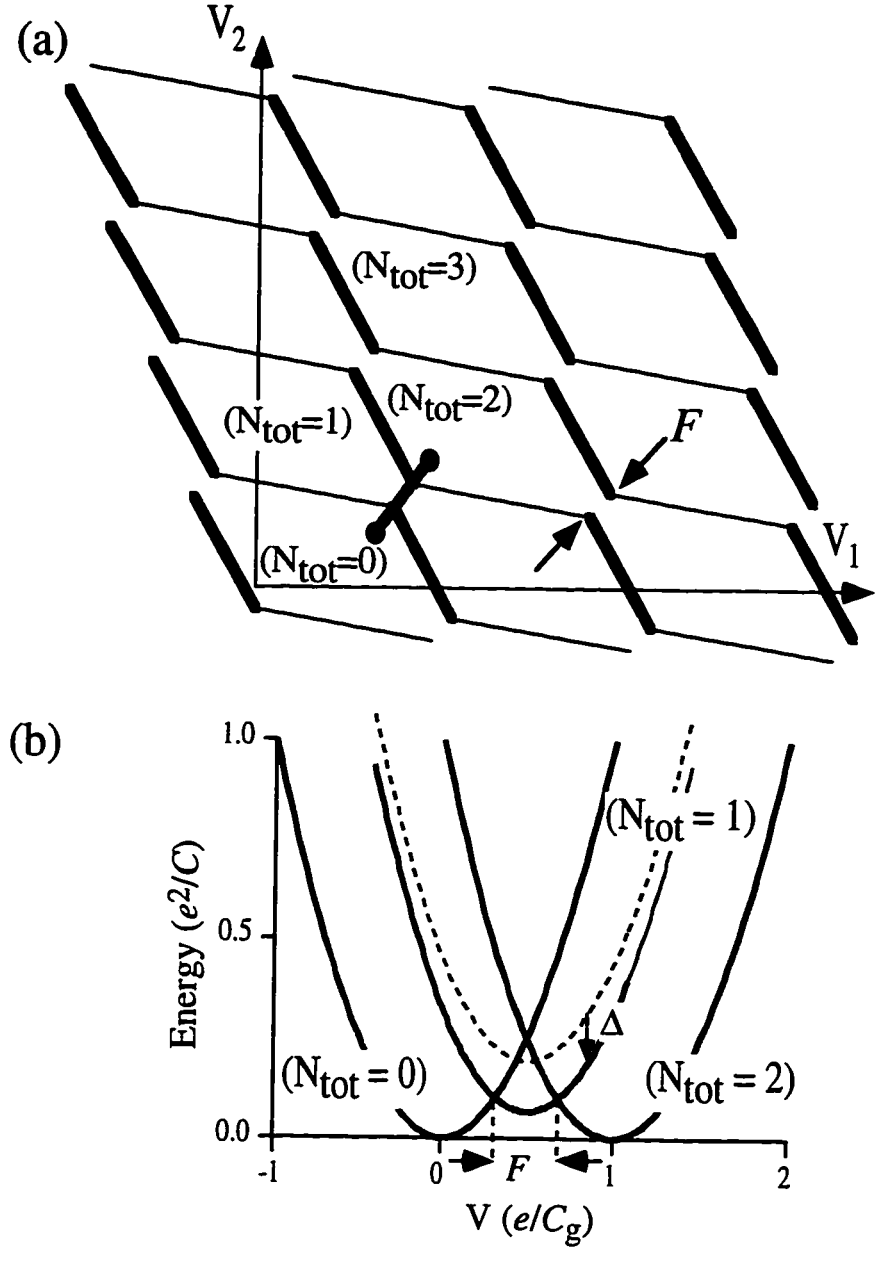


Fig. 3.6 (a) Charging diagram for coupled dot system with finite interdot tunneling showing the splitting F between adjacent columns. N_{tot} remains a good quantum number. (b) The electrostatic energy $W(N_{tot})$ along the dark line segment shown in (a), depicting the downward shift Δ of the $N_{tot} = 1$ ground state energy parabola relative to the zero-tunneling energy parabola, shown as the dashed curve.

minimum potential energy is periodic in ρ with a period of two, the problem need only be solved for ρ in the interval [0,1].

In the weak-coupling limit, $G_{int} << 2e^2/h$, Golden et al. [Golden and Halperin, 1996] use Rayleigh-Schrodinger perturbation theory to calculate the second-order shift in the ground state energy between the ρ = 0 and ρ = 1 states. The result for the splitting F as defined in Figs. 3.6(a) and (b) will be expressed as a fractional splitting f, which is the absolute splitting F normalized to its maximum saturation value. In this weak coupling limit of $G_{int} << 2e^2/h$ the the functional form for f is predicted to be

$$f(G_{\text{int}}) \equiv \frac{4\ln 2}{\pi^2}\frac{G_{\text{int}}}{G_o} + 0.2590\left(\frac{G_{\text{int}}}{G_o}\right)^2 \qquad (3.30)$$

where $G_o \equiv 2e^2/h$.

In the strong interdot tunneling limit where there is nearly one full spin degenerate channel connecting the two dots $G_{int} \rightarrow 2e^2/h$, the techniques based on simple perturbation theory used to derive Eqn. (3.30) are not applicable. The treatment of this limit involves an approach based on a Tomonaga-Luttinger theory, in which the interdot coupling is modeled as a one-dimensional channel with a slightly reflective potential barrier. The shifts in the ground state energies are calculated perturbatively in r, where r is the reflection coefficient in the interdot channel, $0 \le |r| \le 1$, and $G_{int} = 2e^2/h\ (1 - |r|^2)$ [Flensberg, 1993; Flensberg, 1994; Matveev, 1995]. The result in the strong coupling limit $G_{int} \rightarrow 2e^2/h$ is

$$f(G_{\text{int}}) = 1 + \frac{16e^{\gamma}}{\pi^3}\left(1 - \frac{G_{\text{int}}}{G_o}\right)\ln\left(1 - \frac{G_{\text{int}}}{G_o}\right) - 0.4251\left(1 - \frac{G_{\text{int}}}{G_o}\right) \qquad (3.31)$$

where $\gamma \equiv 0.577$ is the Euler-Mascheroni constant.

The calculations presented thus far have not incorporated the constant geometric interdot

capacitance C_{int}. Golden and Halperin [Golden and Halperin, 1996] show that introduction of a constant interdot capacitance results in a simple rescaling of the fractional splitting f such that the fractional splitting f_c for a system with a finite interdot capacitance is related to f by the equation

$$(1-f_c)=\frac{C}{C+2C_{int}}(1-f) \tag{3.32}$$

where C is the total capacitance of each quantum dot.

CHAPTER IV

Experimental Results for Parallel Coupled Quantum Dots

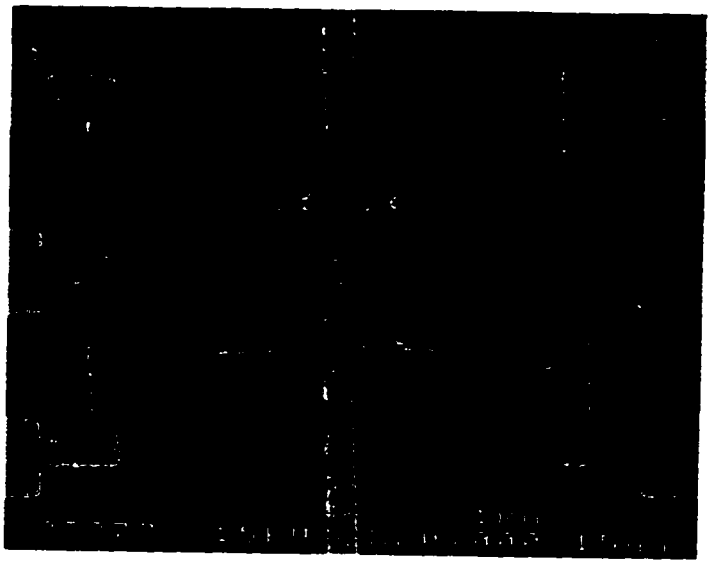
4.1 Introduction

This chapter details low temperature conductance measurements performed on a parallel coupled quantum dot device in the Coulomb blockade regime. The experiments are designed to probe explicitly the role of quantum mechanical interdot coupling in the coupled dot system. The device is realized in a two-dimensional electron gas using tunable electrostatic surface gates which allow a large degree of control over the various tunnel barriers and confining walls which define the quantum dot system. Consequently, before setting out to measure the properties of the double-dot system we characterize the behavior of the different components of the device.

4.2 Device Design

A scanning electron micrograph of the coupled parallel quantum dot device used for the experiments described in this section is shown in Fig. 4.1(a). Figure 4.1(b) is a schematic of the gate layout indicating the labelling convention used. The device consists of two nominally identical adjacent quantum dots of lithographic size $A_{dot} = 0.8\ \mu m \times 0.5\ \mu m$. The dots are defined by eight independently tunable Cr:Au Schottky gates on the GaAs/AlGaAs heterostructure wafer KC7 (whose properties are summarized in chapter 2).

(a)



(b)

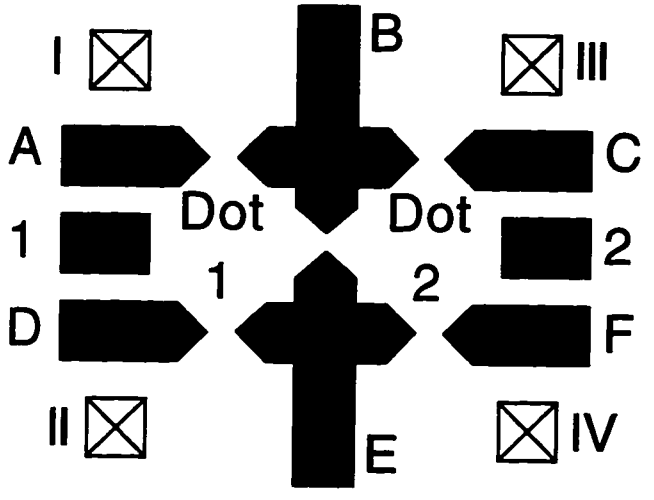


Fig. 4.1 (a) SEM micrograph at 20,000× magnification of the Cr:Au surface gates of a parallel coupled quantum dot device showing 1 μm scale bar. (b) Labeling convention for dots and gates used in the text. G_{ij} refers to the conductance through the QPC formed by gates i, j; G_i corresponds to the conductance through dot i. Ohmic contacts to the 2DEG are denoted by crossed squares.

Each of the metallic gates shown in Fig. 4.1(a) is independently controlled except for gates B and E, which are wired together on the chip. All of the gates extend to the edge of the sample to allow for independent characterization of each of the quantum point contacts and to ensure that there are no conduction paths other than those through the quantum dots. The eight gates define five separately tunable quantum point contacts. The four outer quantum point contacts are used to measure the conductance of each quantum dot, while the inner quantum point contact controls the interdot tunnel-coupling between the dots. The lithographic width of the gap in each point contact is designed to be 150 nm, however due to exposure proximity effects during lithography (see chapter 2) the inner quantum point contact has a slightly larger gap width of approximately 200 nm. The side gates 1 and 2 form the confining walls of each dot and voltages applied to these gates can be used to change the potential of each dot. There are four ohmic contacts to the 2DEG, one at each corner of the device as shown schematically in Fig. 4.1(b) (labelled I, II, III, and IV), which allow measurement of both dots and independent characterization of all five quantum point contacts.

From the lithographic area A_{dot} of each dot we can estimate an upper bound on the number of electrons on each dot of $N \approx n_s A_{dot} = 1500$ electrons per dot. The actual occupancy of each dot will be less than this estimate because the depletion regions induced in the 2DEG extend out from the lithographic limit of each surface gate due to capacitive edge effects. Theoretical study of the electrostatic confining potential induced by the surface gates is a complicated problem which requires a self-consistent solution of the Poisson and Schrodinger equations, and must be solved numerically [Stopa, 1993; Kumar, 1992].

4.3 Quantum Point Contacts

The first step in characterizing the Coulomb blockade parallel quantum dot device involves investigating the properties of each of the quantum point contacts. Shown in Fig. 4.2(a) are conductance traces for the four outer point contacts of the parallel dot device, and Fig. 4.2(b) shows the conductance of the inner quantum point contact, all taken at base temperature of the dilution refrigerator mixing chamber, $T_{mc} \approx 35$ mK. The conductance of the inner quantum point contact G_{BE} was measured as a function of the voltage on gates B and E, which are tied together on the chip, with all other gates grounded. The conductance of outer quantum point contact G_{ij}, defined in Fig. 4.1(b) as the point contact formed by gates i and j, was measured with $V_B = V_E = -1.100$ V and all other gates grounded, using the appropriate pair of ohmic contacts, with the opposite pair of ohmic contacts grounded. For example, G_{AB} is measured by setting $V_B = V_E = -1.100$ V, using ohmic contacts I and II, and grounding all other gates and ohmic contacts. At $V_B = V_E = -1.100$ V, the inner quantum point contact is well beyond pinchoff, as seen in Fig. 4.2(b), and there is no tunneling of electrons across the barrier. This was further verified by noting that with $V_B = V_E = -1.100$ V a bias voltage of 0.2 V was required across ohmic contacts I and III before a current of 1 pA was measured.

Although all four outer quantum point contacts are nominally identical in lithographic design, major variations in the conductance properties of each are evident from Fig. 4.2(a). Perhaps most significant for the purposes of the experiments described here is the range in pinchoff voltages at which the conductance of each point contact reaches zero, since for Coulomb blockade experiments the quantum point contact barriers to the dot are set to the low conductance tunneling regime. The pinchoff voltages for the set of quantum point contacts vary from -1.4 V to -1.8 V, demonstrating the necessity for independent control over each quantum point contact. This range in quantum point contact pinchoff voltages is

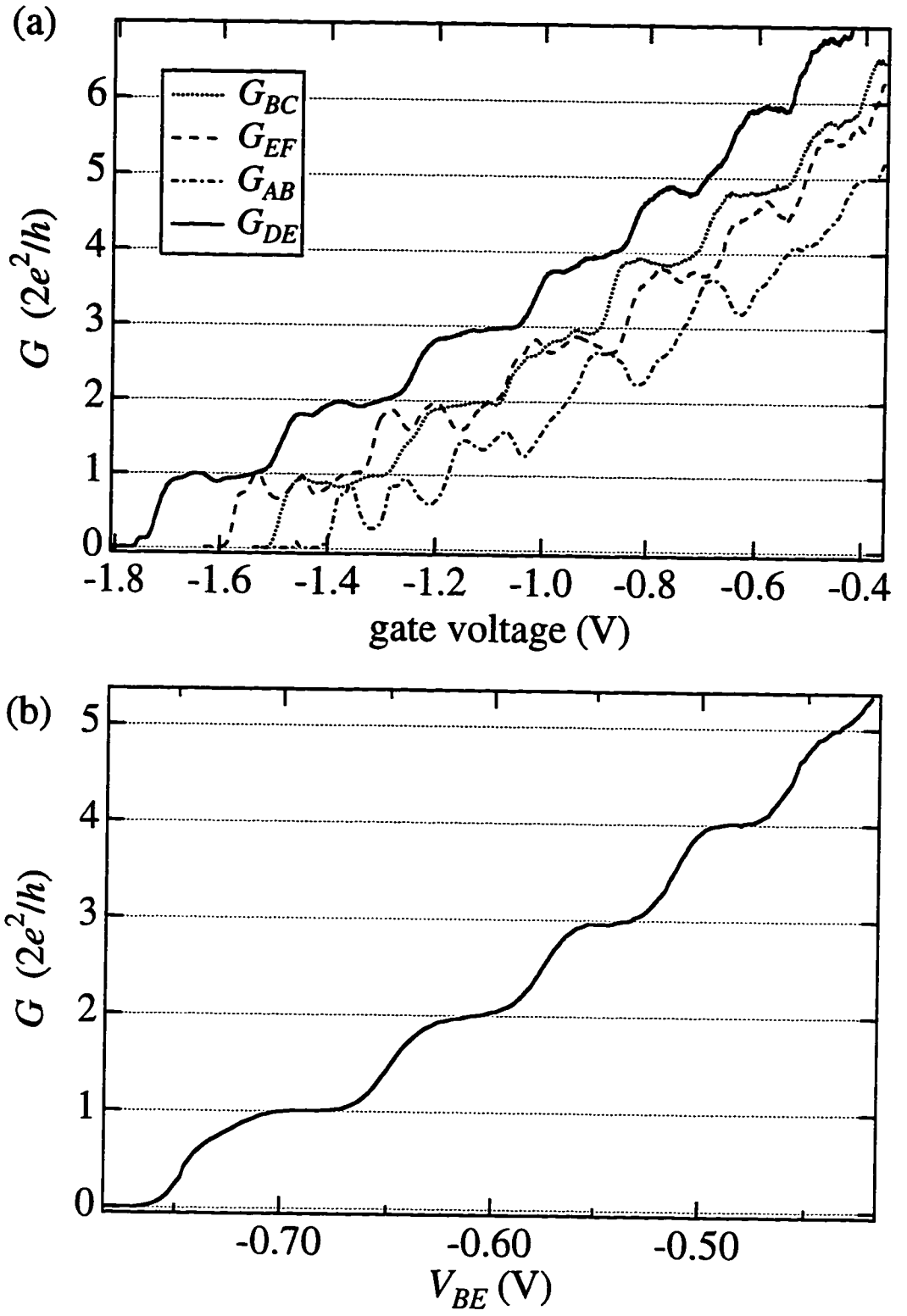


Fig. 4.2 (a) Conductance G vs. gate voltage for the four outer quantum point contacts of parallel dot device, measured at 30 mK. For all traces, $V_B = V_E = -1.1$ V, and the gate being swept is A, C, D, or F with all other gates grounded. (b) G vs. gate voltage V_{BE} for the inner quantum point contact connecting the two quantum dots.

primarily due to nonuniformities in the 2DEG carrier density arising from the disordered impurity potential [Haanappel and van der Marel, 1989; Nixon, Davies and Baranger, 1991; Laughton *et al.*, 1991], impurities or imperfections in the surface Schottky gates, or damage to the 2DEG from electron-beam exposure during lithography [Ghanbari *et al.*, 1992].

Another dramatic feature of the quantum point contact conductance traces in Fig. 4.2(a) is the additional structure on the conductance plateaus. Calculations [Szafer and Stone, 1989] show that such oscillatory structure on the conductance steps is due to transmission resonances associated with reflections at the entrance and exit of the point contact constriction which periodically depress the conductance below its quantized value. Backscattering of electrons from the exit of the constriction is a result of the non-adiabatic abrupt nature of the ends of the point contact channel. Resonant transmission of the reflected electrons occurs when the constriction length is approximately an integer multiple of half the electron longitudinal wavelength in the channel, leading to oscillations on top of the conductance plateaus. Detailed comparison with theory is difficult, because the properties of the transmission resonances are very sensitive to the precise shape of the quantum point contact confining potential and the impurity potential in its vicinity. Finally, we note that significant oscillatory structure in the conductance data of Fig. 4.2(b) for the inner quantum point contact is absent, suggesting that the geometry of the outer quantum point contacts induces a more abrupt confining potential than that produced by gates B and E which define the inner point contact.

Also seen on some quantum point contact conductance traces are sharp isolated peaks located near the pinchoff point of the first conductance step. Such a series of peaks is shown in Fig. 4.3(a), which is conductance data taken at $T_{mc} \approx 35$ mK for the quantum point contact formed by gates A and B, with $V_B = V_E = -1.100$ V as before, and all other gates grounded. We attribute these peaks to resonant tunneling through a single impurity

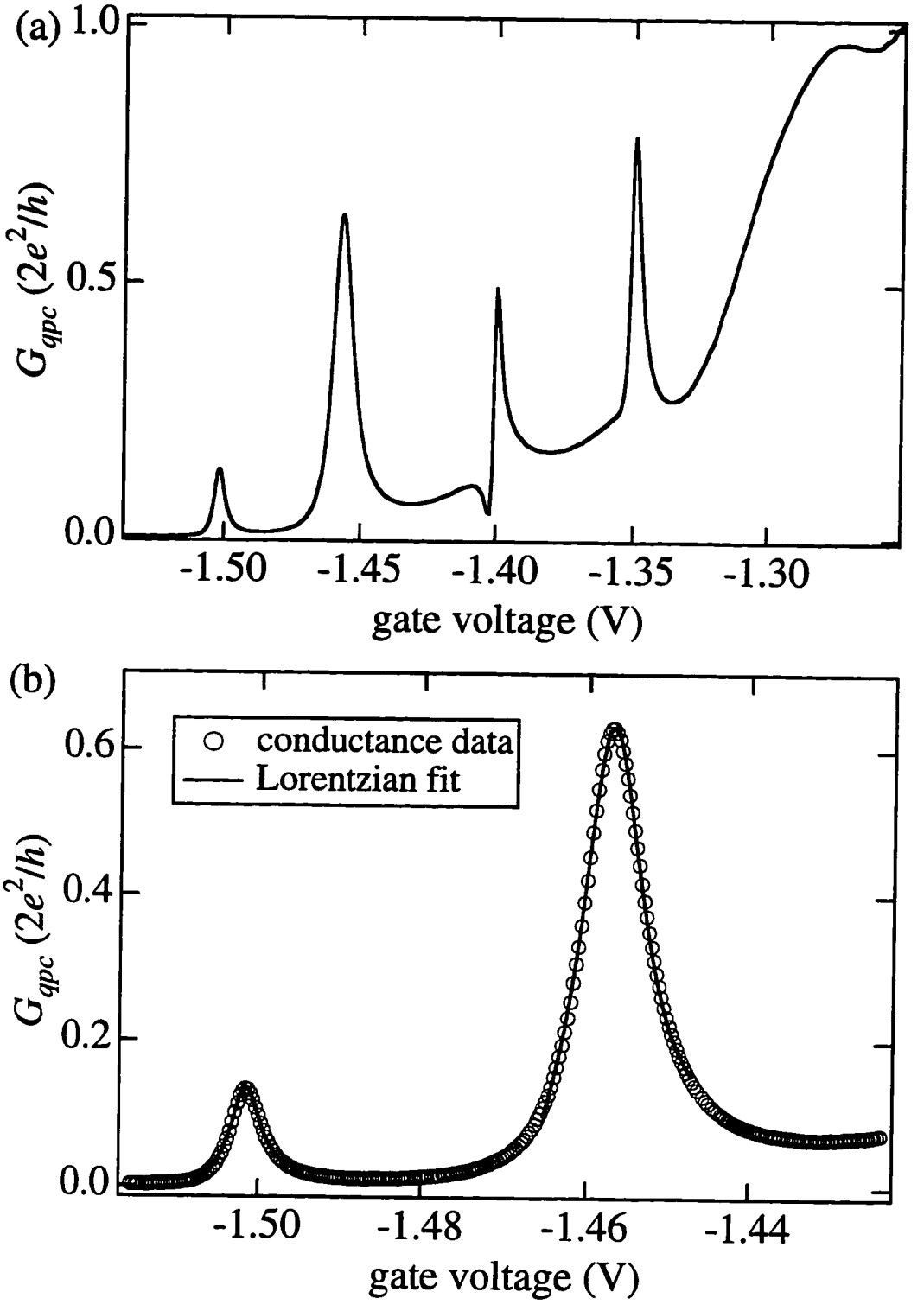


Fig. 4.3 (a) QPC conductance G_{qpc} vs. gate voltage at 30 mK showing four transmission resonances on the first conductance step. (b) Close-up of two of the conductance resonances together with Lorentzian fits to both peaks.

ion in the quantum point contact channel. Such transmission resonances have been previously studied in narrow channels theoretically [Xue and Lee, 1988; Chu and Sorbello, 1989; Masek *et al.*, 1989] and experimentally [Kopley, 1988; McEuen *et al.*, 1990]. If the resonances are well separated in energy, a single state will give the dominant contribution to the transmission coefficient. The conductance G as a function of the Fermi energy E_F through a single localized state is given by the Breit-Wigner formula, and has a Lorentzian lineshape centered about the resonance energy E_o of the impurity state

$$G(E_F) = \frac{e^2}{h} \frac{\Gamma_L \Gamma_R}{(E_F - E_o)^2 + (\Gamma_L/2 + \Gamma_R/2)^2} \tag{4.1}$$

where $\Gamma_L/\hbar$ and $\Gamma_R/\hbar$ are the tunneling rates out of the resonance to the left and right respectively. Fig. 4.3(b) is a close-up of the first two measured transmission resonances of Fig. 4.3(a) fit to a curve which is the sum of a Lorentzian and a term linear in gate voltage to account for the rising background as the first conductance step is turned on. At finite temperatures, the measured conductance is the convolution of Eqn. (4.1) and the energy derivative of the Fermi distribution function. To a first approximation, the full width at half maximum Γ of such a thermally broadened resonance peak will be given by the sum of the width of the zero-temperature peak, $\Gamma_L + \Gamma_R$, and the width of the derivative of the Fermi function, 3.5 $k_B T$. For an order of magnitude estimate of the tunneling rates we assume an electron temperature of 100 mK, and a conversion factor between the gate voltage and the Fermi energy in the constriction of dV_g/dE_F = 10 mV/meV, and find $(\Gamma_R/\hbar + \Gamma_L/\hbar) \approx 10^{12}$ s^{-1}.

Shown in Fig. 4.4 are traces of the conductance of three quantum point contacts as a function of time with each initially set to $G(t = 0) \approx .026\ e^2/h = (1\ \text{M}\Omega)^{-1}$, which is a typical barrier conductance used for the Coulomb blockade experiments described later in this chapter. Also shown for comparison purposes in Fig. 4.4 is a conductance trace with

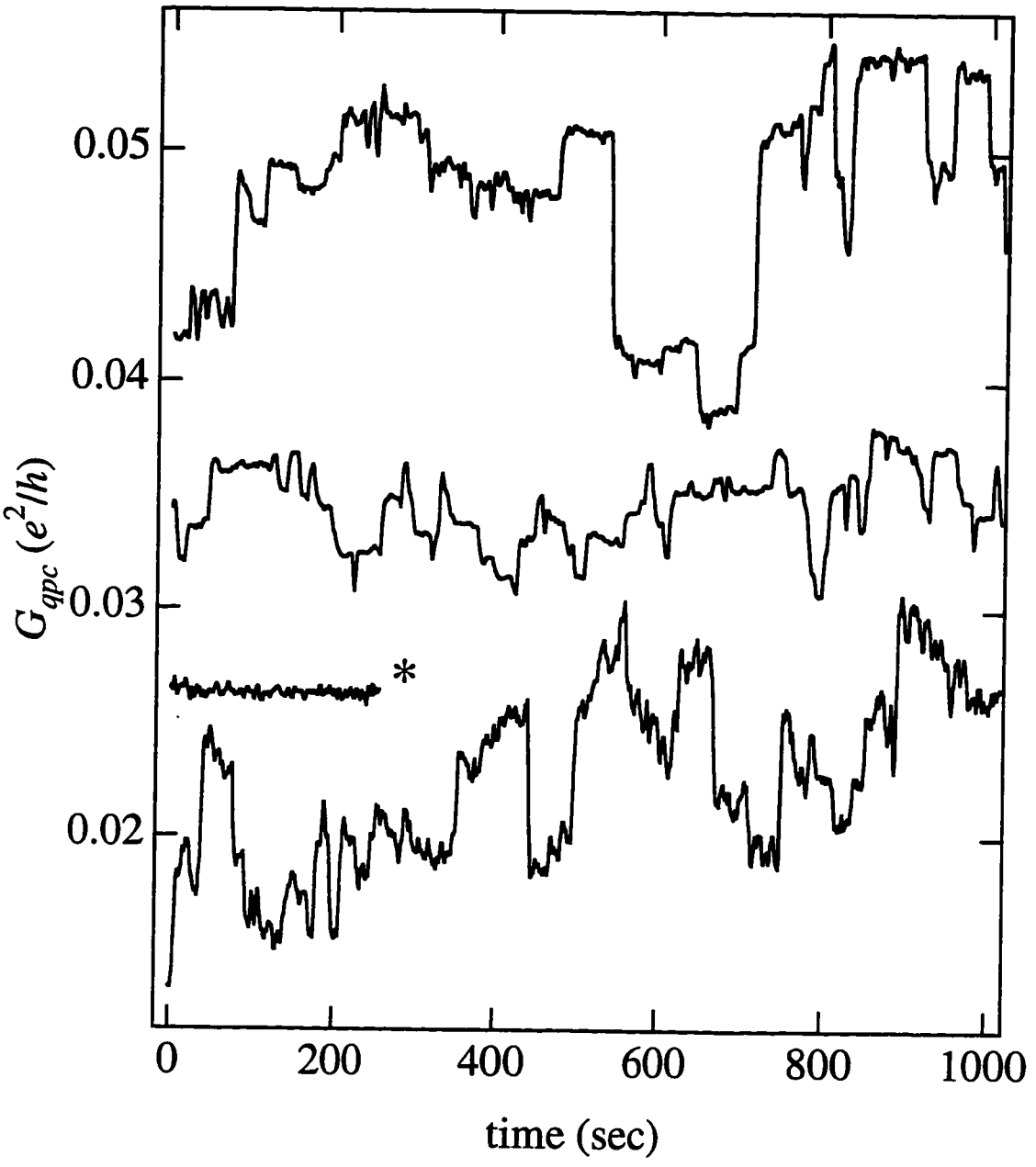


Fig. 4.4 Conductance G_{qpc} of quantum point contacts vs. time, measured at 35 mK. All QPCs were initially set to $G(t = 0) \approx .026\ e^2/h$; the traces are offset vertically for clarity. From top to bottom, the curves correspond to G_{AB}, G_{DE} and G_{BC}; the trace marked with an asterisk (*) is the measured conductance of a 1 MΩ calibration resistor external to the experiment.

a 1 MΩ calibration resistor in the circuit in place of the sample. As can be seen, each of the quantum point contacts exhibits random telegraph-noise-like switching between different differential conduction states. The time scale for a switching event is seen to be approximately 50 seconds, with a wide distribution of faster and slower events. Similar conduction instability has been observed in split gate quantum dots [Wu *et al.*, 1992; Ralls *et al.*,1993] and narrow channels [Cobden *et al.*, 1991]. Proposed origins of the conduction switching instability include trapping and detrapping of electrons from single localized impurity sites near the constriction, and ionization and de-ionization of DX centers near the point contact region. The result of both of these processes is to induce fluctuations in the confining potential of the quantum point contact channel, modulating the measured transport conductance. The quantum point contact behavior exhibited in Fig. 4.4 was characteristic of the device used to produce the results presented in this thesis. Switching events on a time scale of tens of seconds or shorter were typically observed in Coulomb blockade conductance data traces presented in this chapter (see section 4.5.1).

4.4 Single Quantum Dots

Before performing experiments on the double quantum dot device, we first separately measure the characteristics of each individual quantum dot. Shown in Fig. 4.5(a) is the single-dot conductance G_1 of dot 1 as a function of the gate voltage V_1 on side gate 1, taken at the base temperature of the dilution refrigerator mixing chamber $T_{mc} \approx 35$ mK. For single-dot measurements of dot 1, gates C, 2, and F, which are used to define dot 2, are grounded, as are ohmic contacts III and IV; G_1 is then measured using ohmic contacts I and II. The voltages on gates B and E are set to $V_B = V_E = -1.100$ V to ensure that there is no leakage of electrons across the inner quantum point contact barrier, as discussed

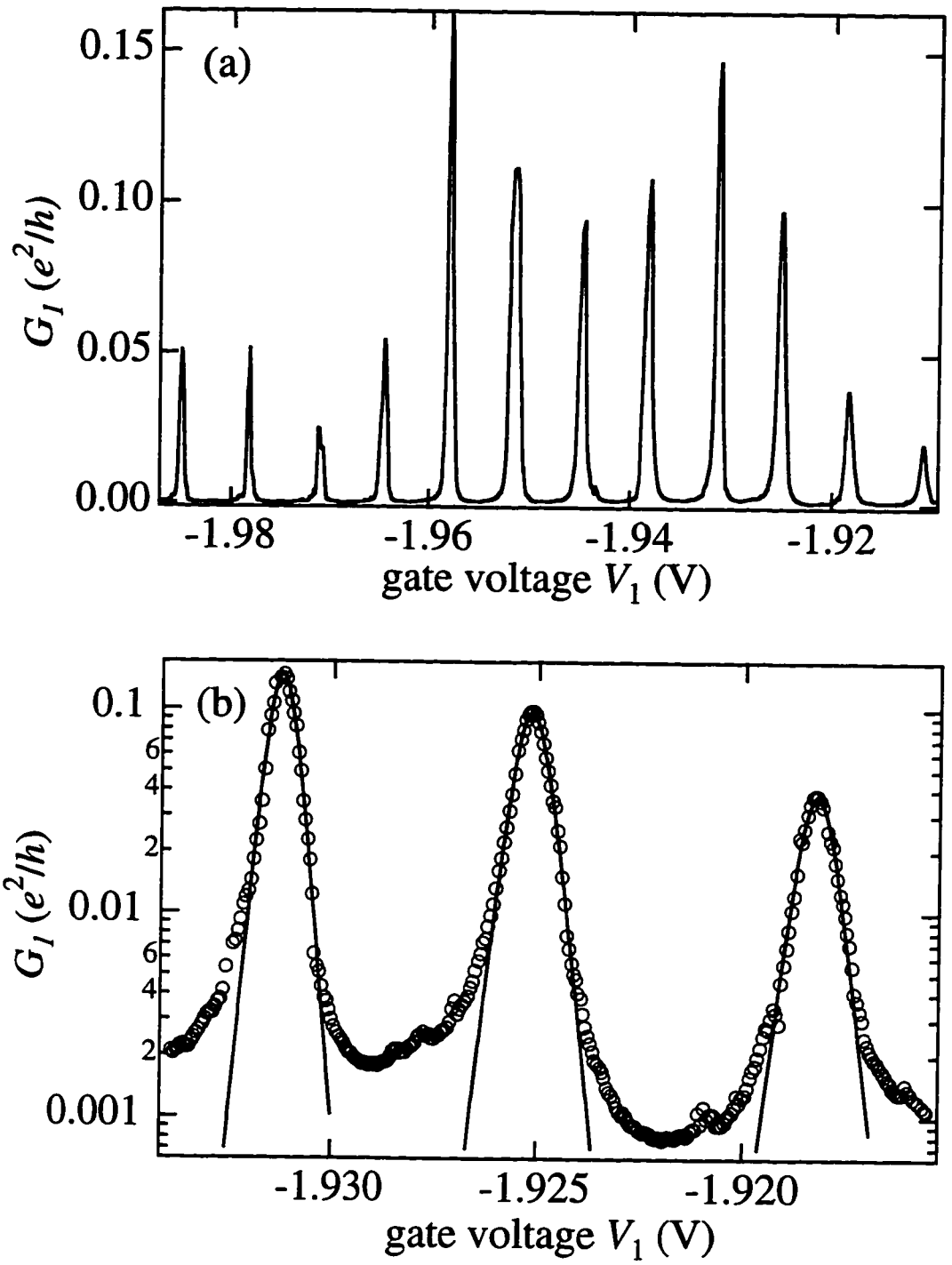


Fig. 4.5 (a) Conductance peaks of dot 1 vs. gate voltage V_1. (b) Close-up view of three peaks from (a) on log scale (open circles), together with fits to thermally broadened lineshape of Eq. (3.20) (solid line).

in the previous section. The quantum point contacts which control the tunnel barriers to dot 1 are set to $G_{AB} \approx G_{DE} \approx 0.02\ e^2/h$. This value is necessarily only an estimate of the actual point contact conductances, since it is not possible to make a measurement after the other gates defining the dot have been energized, and has been arrived at accounting for the influence of adjacent gates (see Sec. 4.5.1). The data of Fig. 4.5(a) show regularly spaced Coulomb blockade conductance peaks as a function of gate voltage with a period $\Delta V_g \approx$ 7.1 mV. From Eqn. (3.16), the Coulomb blockade peak periodicity for dot j measured by sweeping the voltage on gate i is determined both by the level spacing ΔE and the capacitance $C_{\text{i,dot j}}$ of gate i to dot j. As discussed in chapter 3, for the experiments described in this thesis the level spacing $\Delta E \approx 50$ μeV is much smaller than the observed peak period of 7.1 mV and can be neglected in a lowest-order approximation for calculating gate capacitance values. With this approximation, the capacitance of gate 1 to dot 1 is calculated to be $C_{\text{1,dot 1}} \approx e/\Delta V_g = 22$ aF.

Fig. 4.6(a) shows a single-dot measurement of the conductance G_2 of dot 2 as a function of the voltage on gate 2. Similar to the measurement for dot 1 described above, here $V_B = V_E$ = -1.100 V, and gates A, 1, and D are grounded as are ohmic contacts I and II. From the measured Coulomb blockade peak period of $\Delta V_g \approx 7.0$ mV for dot 2, we calculate a capacitance between dot 2 and gate 2 of $C_{\text{2,dot 2}} = 23$ aF. Not surprisingly, this is very similar to the value for $C_{\text{1,dot 1}}$, since lithographically both dots are nominally identical. Figure 4.6(b) shows the conductance of dot 2 when the voltage on the far side gate, gate 1, is swept, once again with $V_B = V_E$ = -1.100 V and gates A, D and ohmic contacts I, II grounded. Consistent with Eqns. (3.16) and (3.20), the conductance data exhibit broader and longer period oscillations than in Fig. 4.6(a) due to the smaller dot-gate capacitance in this case. Clearly evident on the Coulomb blockade oscillations is the effect of switching noise (see Sec. 4.3) which randomly and unreproducibly modulates the amplitude of the conductance on the peaks. Estimating the period of the oscillations,

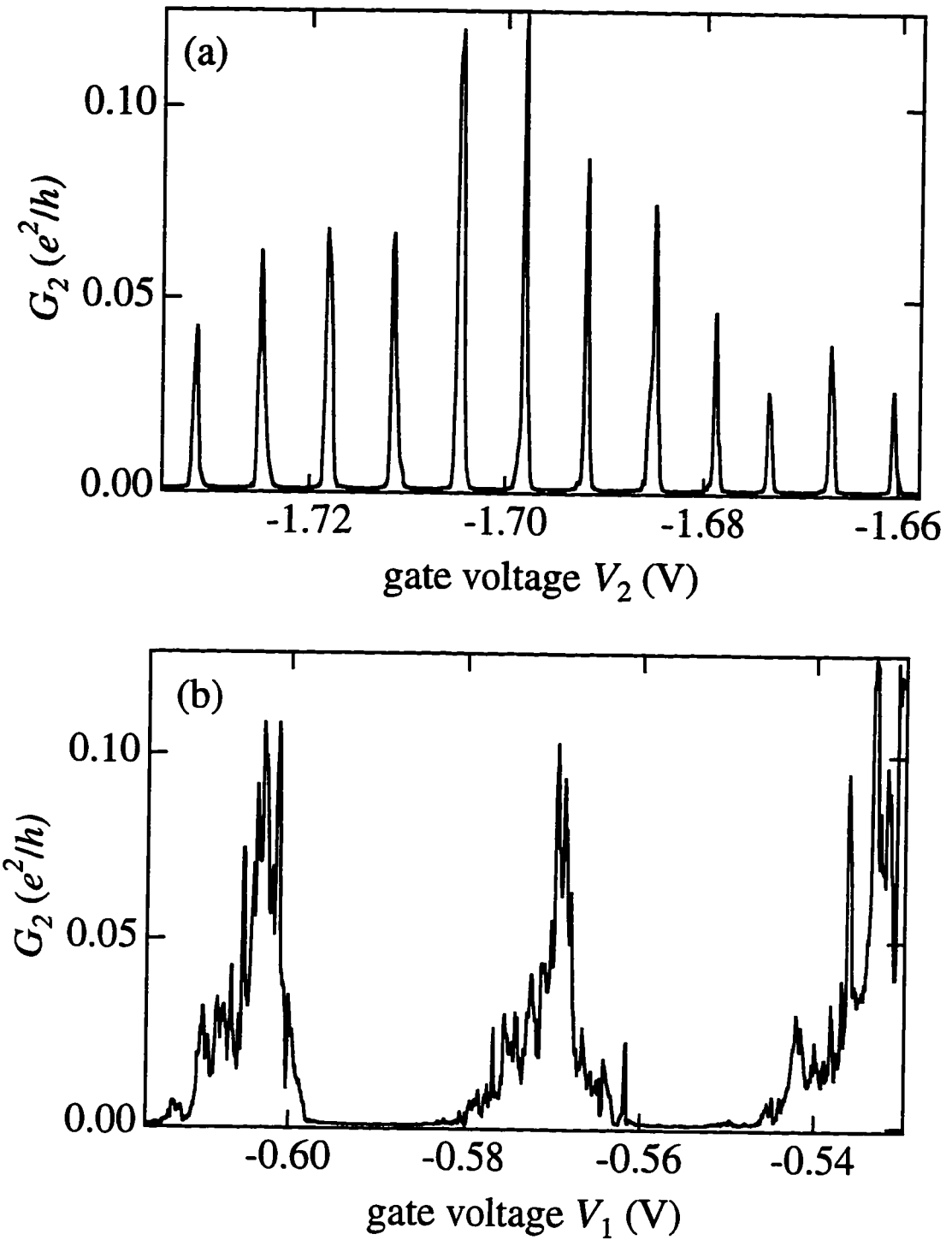


Fig. 4.6 (a) Conductance G_2 of dot 2 vs. gate voltage V_2. (b) Conductance of dot 2 as a function of the gate voltage V_1. The effect of random switching noise on the Coulomb blockade peaks is evident.

$\Delta V_g \approx 32$ mV, we calculate $C_{1,\text{dot } 2} = 5$ aF. Measurements of the conductance through dot 1 as a function of the gate voltage on gate 2 similarly yield $C_{2,\text{dot } 1} = 5$ aF.

The total capacitance and single-particle level spacing for a single dot can be directly measured by applying a finite dc source-drain bias V_{bias} and measuring the differential conductance both as a function of V_{bias} and side gate voltage. Figure 4.7(a) shows a schematic illustration of the potential landscape for a quantum dot containing N electrons under a finite source-drain bias. Here, $V_{\text{bias}} = (\mu_{\text{source}} - \mu_{\text{drain}})/e$, where the states of the source (drain) are fully occupied up to μ_{source} (μ_{drain}). An analysis of the rate equation for the case of finite source-drain bias at zero temperature predicts rhombic-shaped regions where the current flow through the dot is impeded by the Coulomb blockade for voltages satisfying [Grabert and Devoret, 1992]

$$\begin{aligned} e(N - 1/2) &< C_g V_g + (C_{\text{dot-lead } 1} + C_g/2)V_{\text{bias}} < e(N + 1/2) \\ e(N - 1/2) &< C_g V_g + (C_{\text{dot-lead } 2} + C_g/2)V_{\text{bias}} < e(N + 1/2) \end{aligned} \qquad (4.2)$$

where N is the occupancy of the dot and $C_{\text{dot-lead i}}$ is the capacitance between the dot and lead i. This rhombic-shaped Coulomb blockade region is shown schematically in Fig. 4.7(b). As with zero-bias Coulomb blockade conductance oscillations, from Eqn. (4.2) these conductance features in the finite bias regime are seen to be periodic in gate voltage V_g with a period of e/C_g. Physically, for a given gate voltage, the zero conductance regime in V_{bias} is a measure of the Coulomb charging energy of the dot, e^2/C, which must be overcome by the driving voltage before current can flow. Changing the gate voltage corresponds to shifting the bottom of the conduction band and consequently similarly shifts the Coulomb charging gap. At the degeneracy points in gate voltage where the occupancy of the dot fluctuates between N and $N + 1$, the Coulomb blockade is lifted and the current flows for any value of applied V_{bias}. Fig. 4.8(a) is a gray-scale

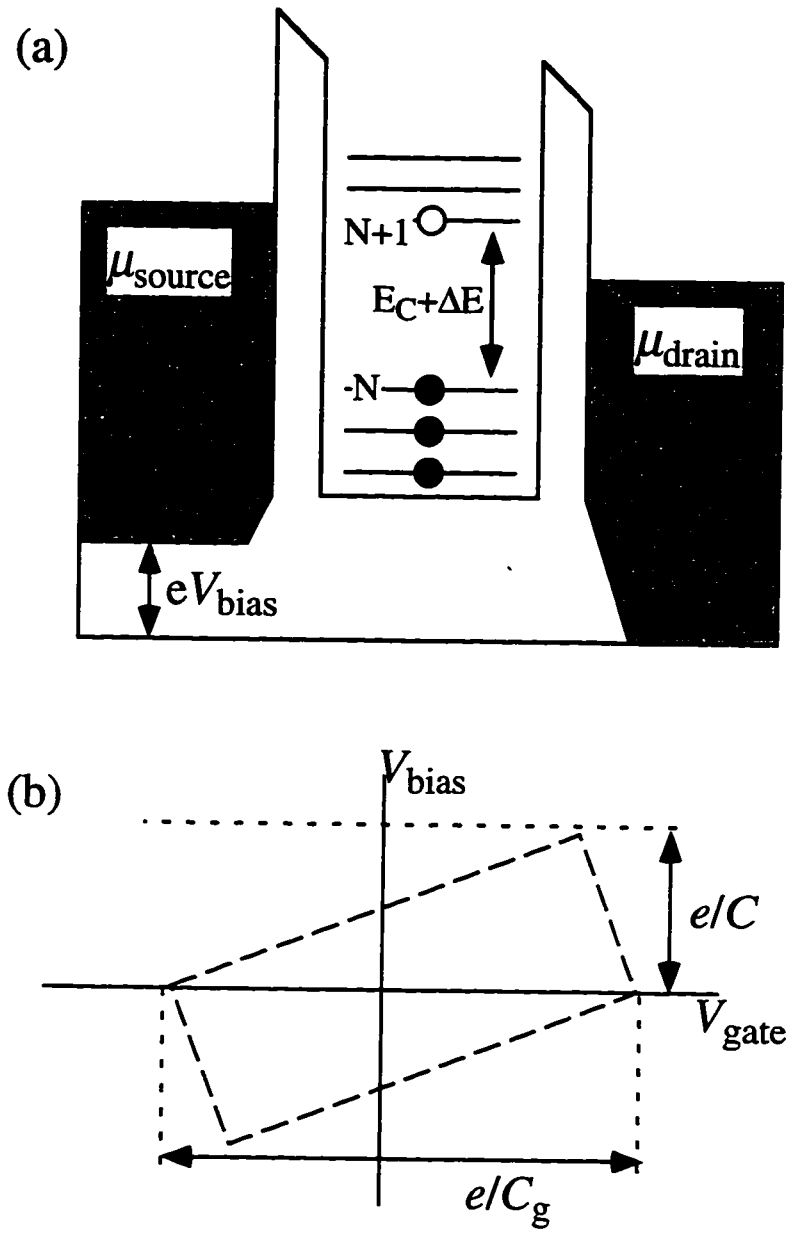


Fig. 4.7 (a) Potential energy landscape for a quantum dot containing N electrons with applied finite voltage bias $eV_{bias} = \mu_{left} - \mu_{right} < \Delta E$. Solid circles denote occupied 0D states. The next available state lies $E_C + \Delta E$ higher in energy. (b) Schematic of rhombic-shaped Coulomb blockade region as determined by the various capacitances. The slope of the rhombus is given by $C_g/(C - C_{dot\text{-}lead})$.

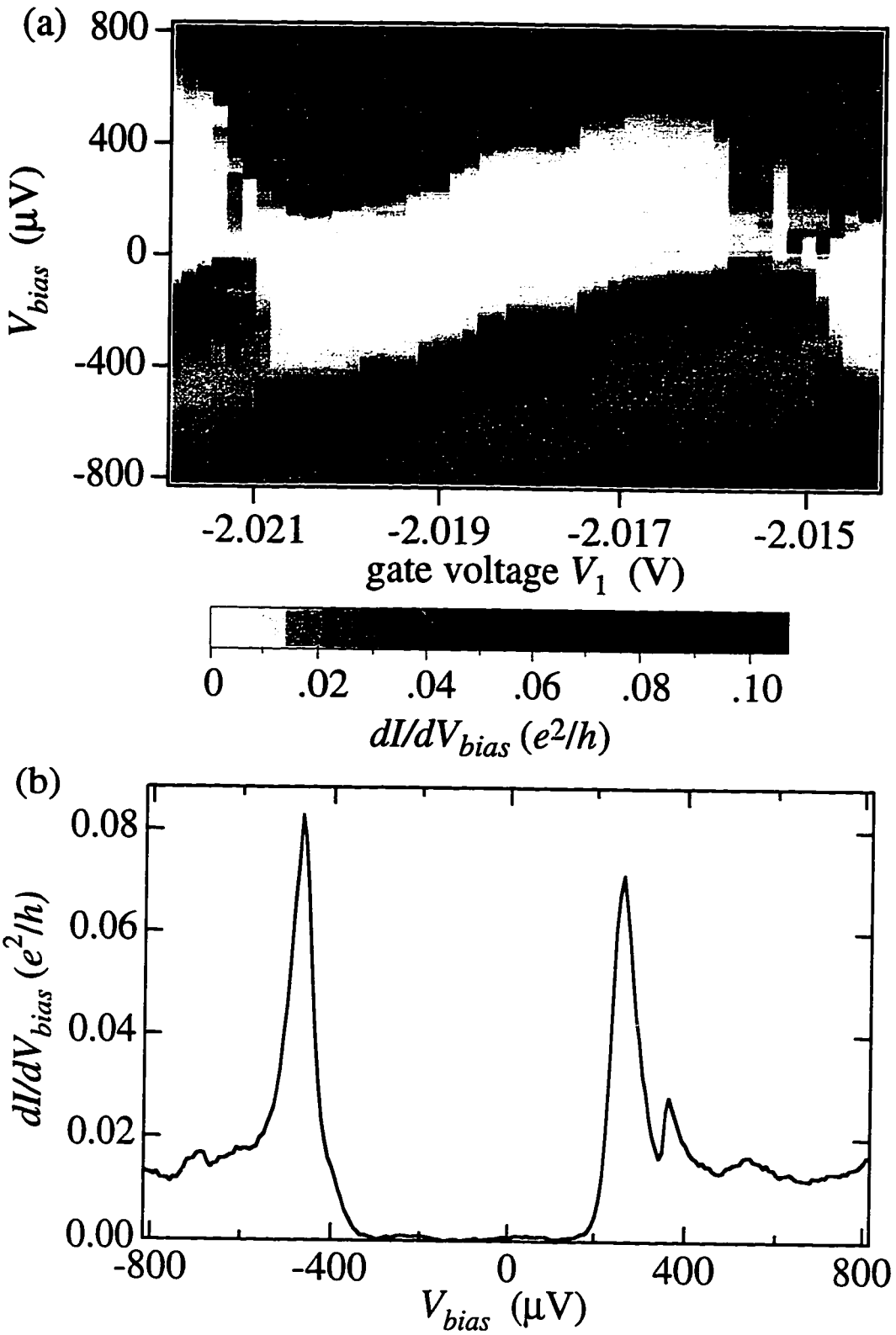


Fig. 4.8 (a) Gray scale representation of differential conductance peaks in the plane of V_{bias} and gate voltage V_1 for dot 1 showing the rhombus-shaped Coulomb blockade region. Dark areas correspond to higher conductance. (b) A representative differential conductance trace dI/dV_{bias} vs. V_{bias} extracted from the data shown in (a) for V_1 = -2.0165 V.

representation of the differential conductance dI/dV_{bias} data from such a measurement for dot 1 as a function of V_{bias} and V_1. The plot consists of 50 sequential traces of dI/dV_{bias} vs. V_{bias}, at discrete values of V_1. One full period of the rhombic shaped region of zero conductance is clearly evident, with parts of adjacent rhombi seen as well. Once again, the effects of switching events in the sample (see Sec. 4.2) are evident in the unreproducible random noise which offsets each adjacent vertical data trace. The single dot total capacitance C determines the vertical height of the Coulomb blockade region and is measured to be C = 320 aF, corresponding to a charging energy of $U = e^2/2C \cong 250$ μeV.

Figure 4.8(b) is a single-dot differential conductance dI/dV_{bias} vs. V_{bias} trace extracted from Fig. 4.8(a) for V_1 = -2.0165 V. The Coulomb gap is clearly seen as the region of zero differential conductance. The additional structure on either side of the Coulomb gap is attributed to the existence of single particle states on the quantum dot. As illustrated in Fig. 4.7(a), the number of current carrying states in the energy interval eV_{bias} increases as V_{bias} is increased, leading to a larger transition rate and consequently more current. The onset of each additional current carrying state leads to peaks in the differential conductance as a function of V_{bias}. Two such peaks are seen to the right of the Coulomb gap in the data of Fig. 4.8(b), at V_{bias} = 380 μV and 540 μV. The average separation between adjacent single particle states is estimated from Fig. 4.8(b) to be $\Delta E \sim 50$ μeV. This value corresponds well with the inferred value of $\Delta E \sim E_F/N \approx 10$ μeV, using E_F = 14 meV and N = 1500 electrons.

As discussed in Chapter 3, the lineshape of the zero-bias single-dot Coulomb blockade conductance oscillations as a function of gate voltage V_g is determined by the relative sizes of the electron temperature T_e, the average level spacing ΔE, and the Coulomb charging energy $e^2/2C$; the experimental values are 13 μeV, 50 μeV, and 320 μeV respectively. Since $k_B T_e < \Delta E < e^2/2C$, the appropriate peak shape is given by Eqn. (3.19), which

depends on the total dot capacitance C, the capacitance between the swept gate and the dot C_g, and the electron temperature T_e. Figure 4.5(b) shows a fit of the single-dot conductance G_1 of dot 1 at base temperature of the dilution refrigerator to the thermally broadened lineshape of Eqn. (3.19). The full-width at half-maximum (FWHM) of the experimentally measured peaks is approximately 0.6 mV, which corresponds to an electron temperature of T_e of 150 mK. This value of T_e is almost five times higher than the nominal lattice temperature of 30 mK, reflecting the electron-phonon thermal resistance inherent in semiconductor 2DEG samples [Hopkins, 1990; Rimberg, 1992].

Figure 4.9 shows the evolution of the middle Coulomb blockade peak of Fig. 4.5(b) as the temperature of the mixing chamber is increased. The solid lines are fits to the thermally broadened peak shape of Eqn. (3.19). Figure 4.10 summarizes the results of the peak height and lineshape FWHM fits to the data of Fig. 4.9. The solid line in Fig. 4.10 is a fit of the conductance peak maxima to the T^{-1} temperature dependence predicted in Eqn. (3.19), exhibiting fair agreement with theory. The dependence of the conductance peak FWHM data on temperature is seen to be approximately linear, as predicted by Eqn. (3.19b) for a single quantum dot.

4.5 Parallel Coupled Quantum Dots

The measurements presented in this section are made on the double dot device of Fig. 4.1(a) with all of the device gates energized, defining two parallel quantum dots. By adjusting the gate voltage on gates B and E defining the central quantum point contact, we are able to tune the device from a regime in which the two dots are well separated to a regime where the two dots have merged into a single composite dot.

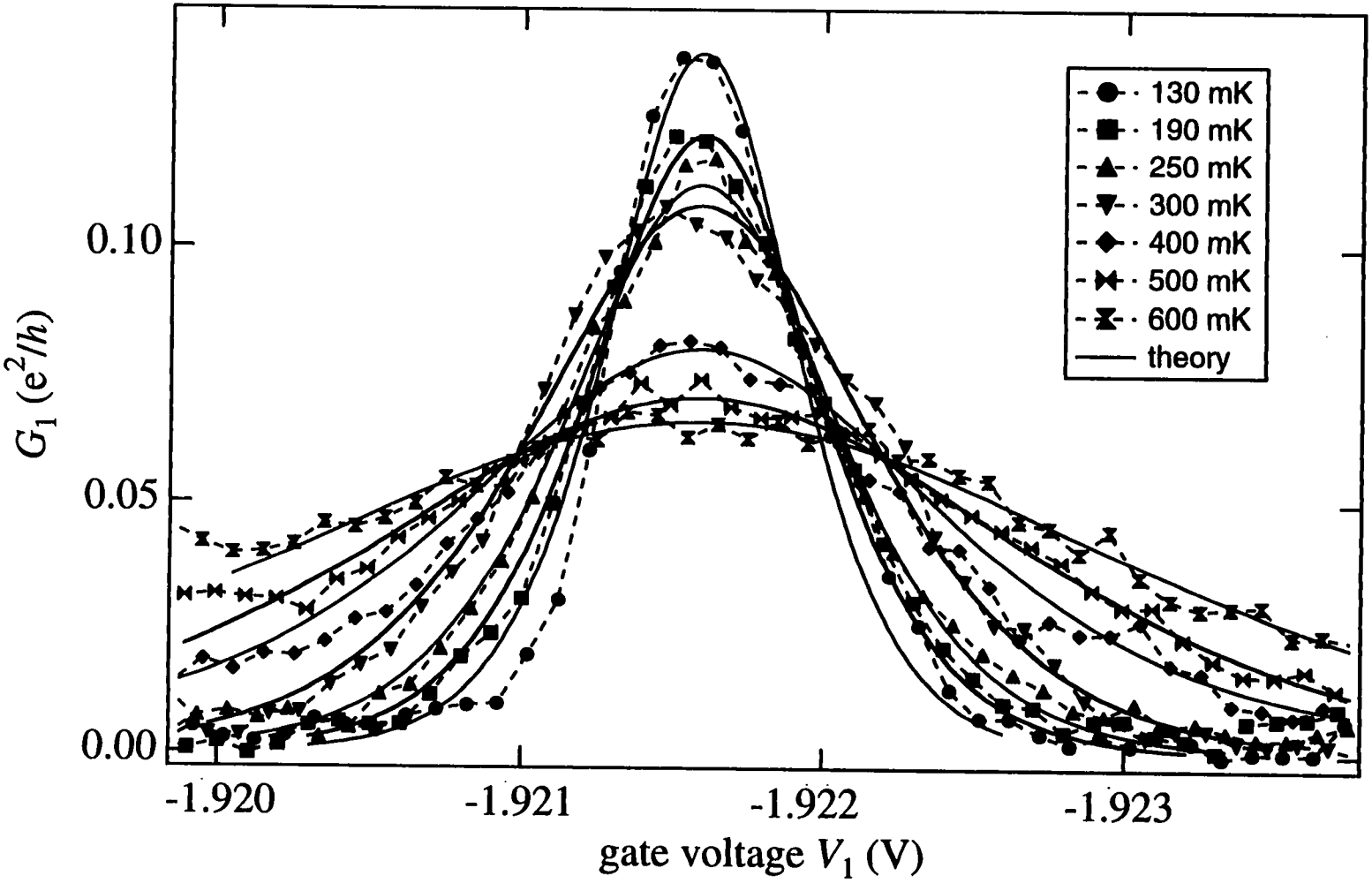


Fig. 4.9 Single-dot conductance G_1 vs gate voltage V_1 for dot 1 at various mixing chamber temperatures. The solid line curves at each temperature are fits to the thermally broadened peak shape of Eqn. 3.19.

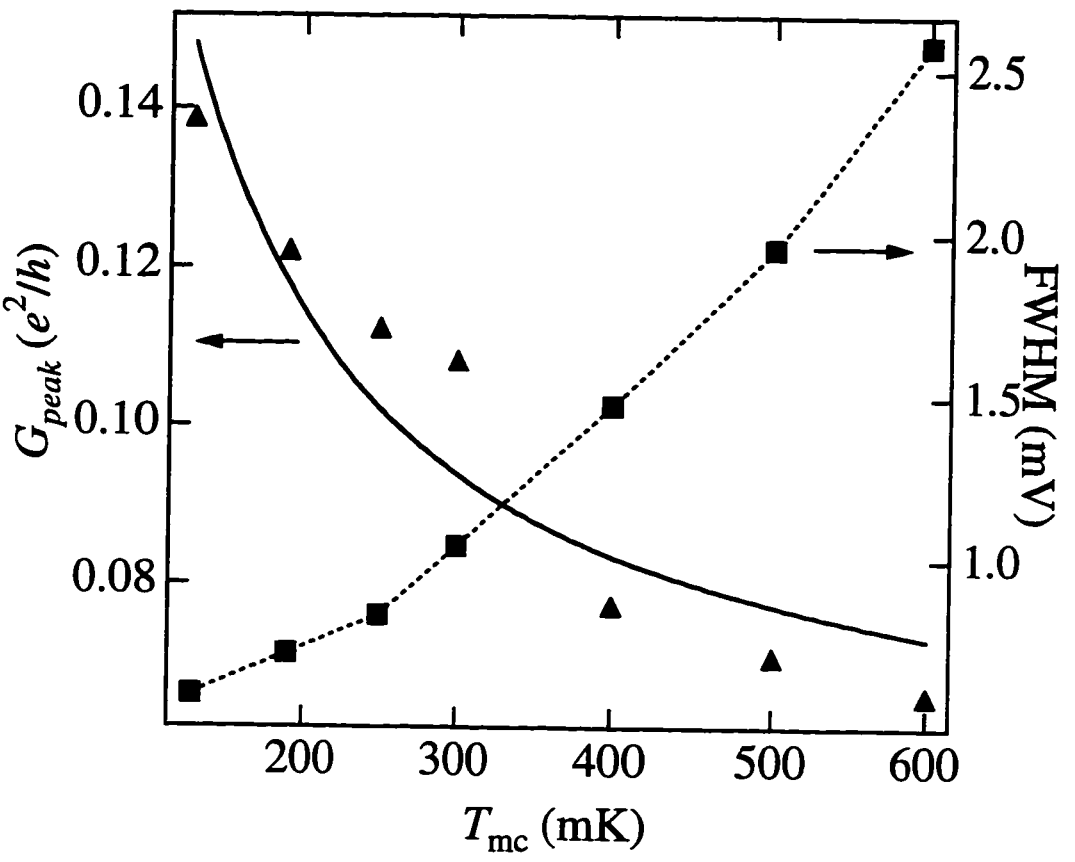


Fig. 4.10 For the peak of Fig. 4.9, peak amplitude G_{peak} (triangles, left axis) and peak full-width at half-maximum FWHM (squares, right axis) vs mixing chamber temperature T_{mc}. The solid line is a fit of G_{peak} to $G_{peak} = \alpha T^{-1}$. Dashed lines are guides.

4.5.1 Measurements with one dot conducting

This section describes the evolution of the Coulomb blockade spectrum of dot 1 as the interdot tunnel coupling, controlled by the inner quantum point contact, is changed. For these measurements, dot 1 is set to be conducting by adjusting its point contacts so that $G_{AB} \approx G_{DE} \approx .02\ e^2/h$, and its conductance is measured using ohmic contacts I and II. Dot 2, however, is well isolated from its leads by setting $G_{BC} \approx G_{EF} \approx 0$. Ohmic contacts III and IV are grounded, as they are not part of the measurement circuit. The interdot conductance, set by the gate voltages $V_B = V_E$, is adjusted as desired between 0 and $2e^2/h$.

Since it is impossible to measure directly the conductance of the inner quantum point contact once all the other gates of the device are energized, a series of initial tests were performed in order to quantify the influence of the other gates on the interdot barrier. Shown in Fig. 4.11 is a set of conductance traces of the inner point contact vs gate voltage $V_B = V_E$, using ohmic contacts I and IV, with other gates on the device energized to approximately the voltage values at which they will be set during the experiment. All of the other gates except A and F can be energized while still monitoring G_{BE}. With gates 1, D, C and 2 energized, the G_{BE} trace is seen to shift by approximately 130 mV toward more positive voltages when compared to the case with all other gates grounded. Energizing only gates C and D moves the G_{BE} curve by 45 mV; therefore, we assume that energizing gates A and F will similarly shift G_{BE} by another 45 mV. The total estimated shift when all other gates are energized is then 175 mV. The conductance trace for the inner quantum point contact, shifted to more positive gate voltage by 175 mV, will be used to estimate the value of the interdot conductance at a given $V_B = V_E$.

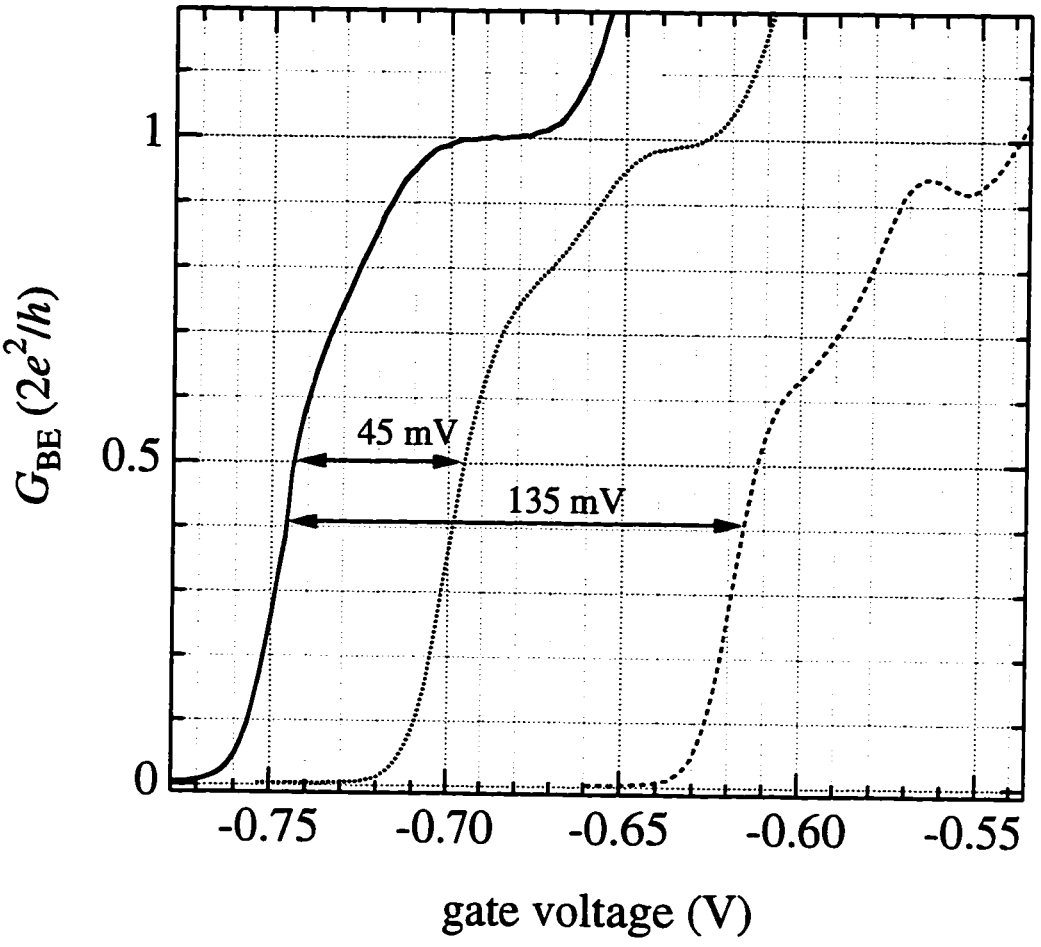


Fig. 4.11 Conductance of inner quantum point contact G_{BE} vs. gate voltage $V_B = V_E$ with all other gates grounded (solid line), with gates D and C energized to -1V (dotted line), and with gates D, C, 1, and 2 energized to -1 V (dashed line).

Charging Characteristics of Parallel Quantum Dot System

We first investigate the regime of low interdot tunnel conductance by setting $V_B = V_E$ = -578 mV, which corresponds to an interdot conductance of $G_{BE} \cong 0.32\ e^2/h$ when the influence of the other gates is taken in to account as described above. Shown in Fig. 4.12(a) is a set of curves of the conductance through dot 1 as a function of the voltage V_1 on side gate 1 at incremented values of the voltage V_2 on side gate 2. Figure 4.12(b) is a gray scale representation of the same data. The pattern of measured conductance peaks exhibits two periodicities, one in each direction of gate voltage. The smaller scale disruptions in peak positions between adjacent data traces are due to switching events in the sample, described in Sec. 4.3, which are seen to occur on a time scale (~ 10 sec) shorter than the time required to complete a single data trace (~ 30 sec). Figure 4.13 shows selected conductance traces extracted from Fig. 4.12.

For the case of very weak interdot conductance as for the data of Fig. 4.12, we expect capacitive interaction between the dots to dominate. It should be emphasized however that the classical capacitive charging model of Fig. 3.4 is not strictly appropriate in this regime, because there is a small but finite interdot tunnel conductance which leads to non-capacitive sharing of electrons between the dots. Nevertheless, as a first step, we will begin our analysis of the data using the classical capacitive charging model of Sec. 3.4.1, and then consider the corrections introduced by the quantum charge fluctuation model presented in Sec. 3.4.2.

The model capacitive charging diagram of Fig. 3.5(a) is seen to qualitatively reproduce the pattern of conductance peaks in the data of Fig. 4.12(b). As described in Sec. 3.4.1, each unit cell corresponds to a different charge state of the coupled dot system, and the boundaries between adjacent cells represent energy degeneracy points where

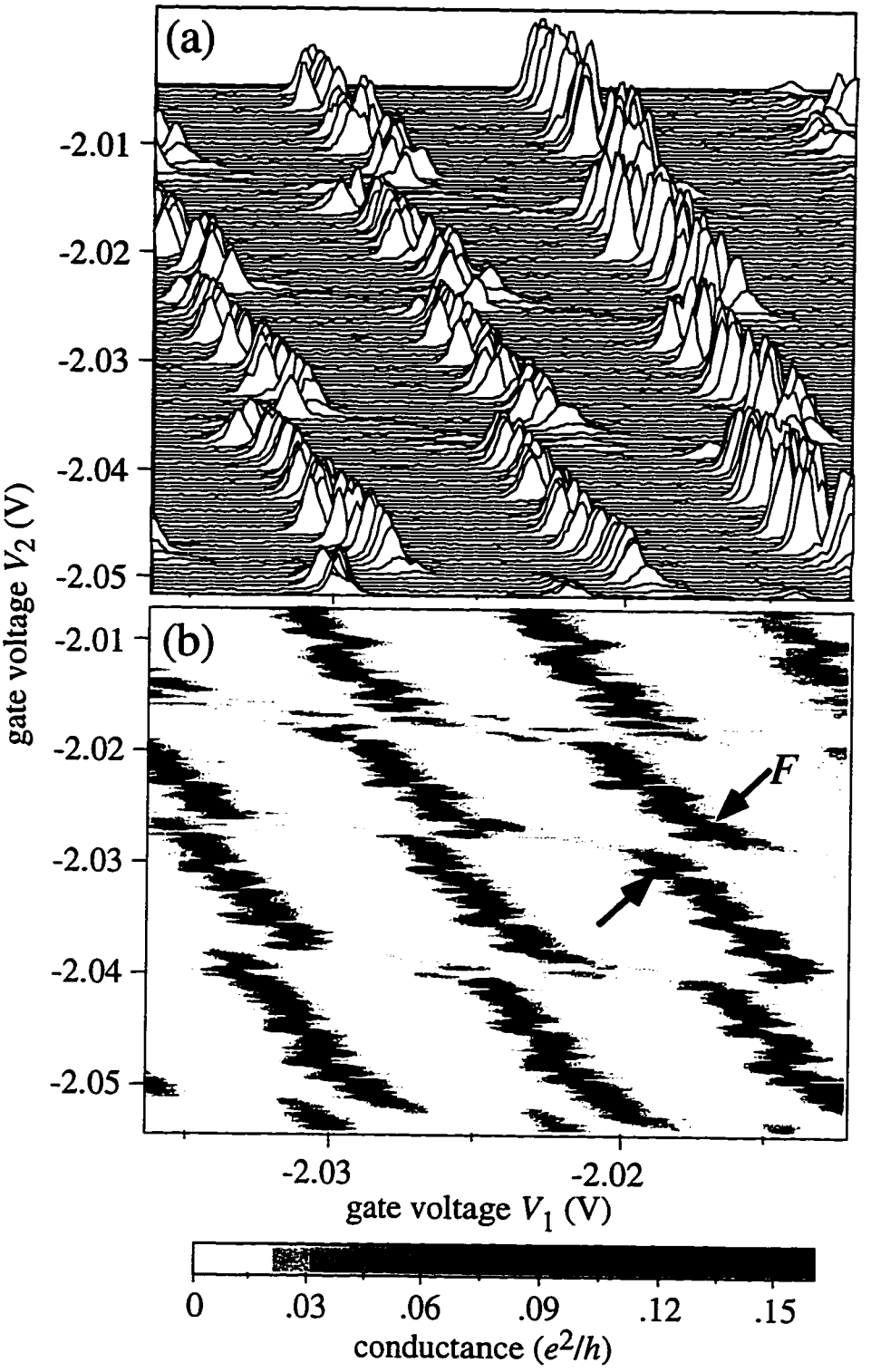


Fig. 4.12 (a) Conductance data for $G_{BE} \approx 0.3\ e^2/h$ as a function of the two side gate voltages V_1 and V_2. (b) Gray-scale representation of the same conductance data, showing the splitting F discussed in the text.

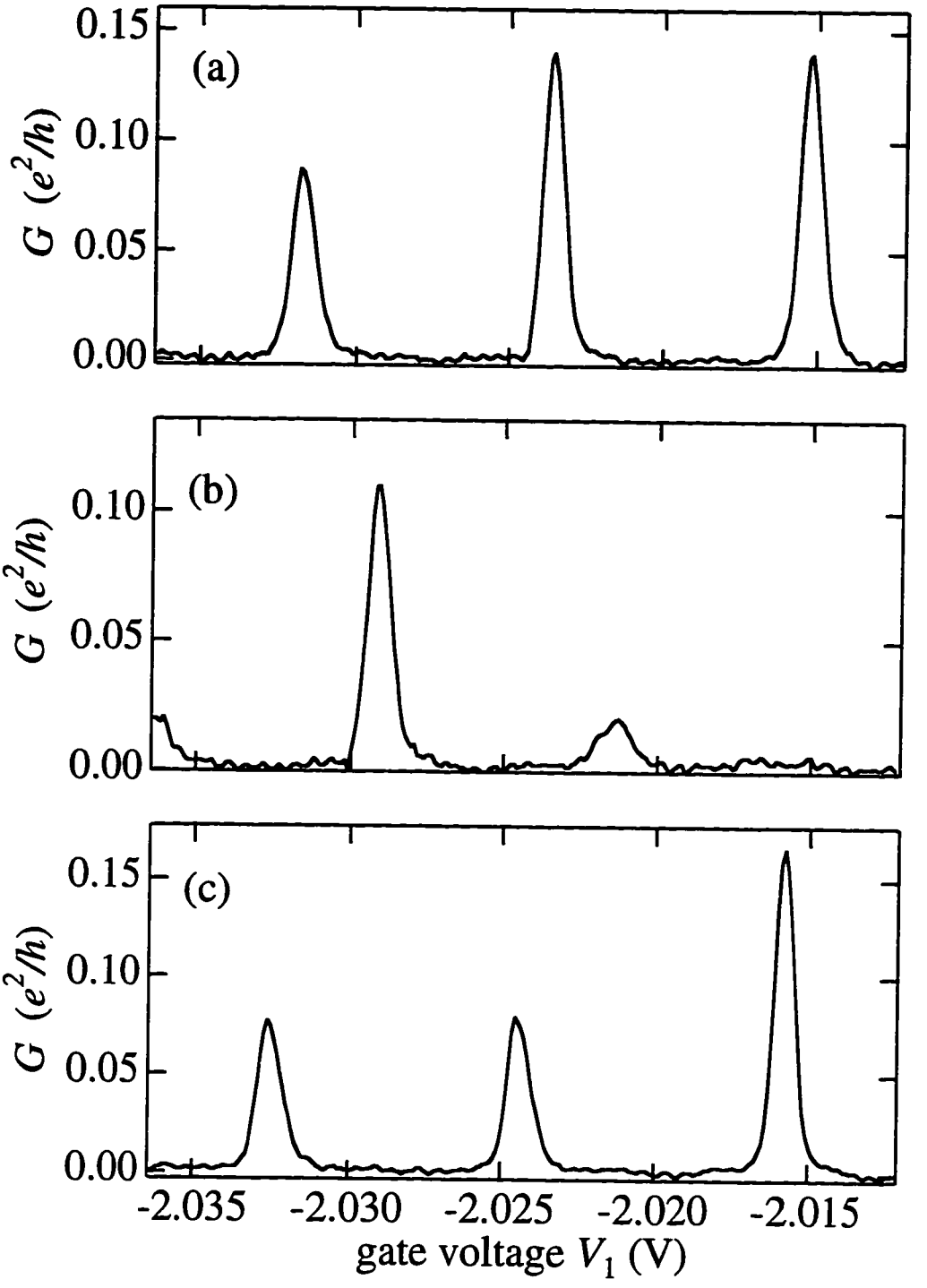


Fig. 4.13 Representative conductance traces extracted from Fig. 4.12 for V_2 = -2.045 V (a), V_2 = -2.036 V (b), and V_2 = -2.023 V (c).

$W(N_1, N_2) = W(N_1 \pm 1, N_2 \pm 1)$. Comparing the data of Fig 4.12 to the charging diagram of Fig. 3.5(b), we see that the large conductance peaks in the data of Fig. 4.12(a), or equivalently the dark regions of Fig. 4.12(b), correspond to changes in the occupancy of the conducting dot (dot 1). The periodicity of the data of Fig. 4.12 in the V_1 direction then reflects single electron charging of dot 1, and determines the capacitance between dot 1 and gate 1. From Eqn. (3.25), and using $C_{1,dot2} = 5$ aF (from Sec. 4.4), we find $C_{1,dot1} =$ 24 aF, consistent with the value of $C_{1,dot1} = 22$ aF obtained without dot 2 defined (Sec. 4.4).

Changes in the occupancy of dot 2, reflected by the periodicity in the V_2 direction, lead to discontinuous jumps in the electrostatic potential which influences dot 1 and result in the periodic abrupt shifts in the phase of the Coulomb blockade peak spectra seen in the data of Fig. 4.12. The appearance of the smaller secondary peaks, seen as the fainter horizontal trends in Fig. 4.12(b) and as the shorter peak of Fig. 4.13(b), reflects a change in the occupancy of dot 2 by one electron and is not explained by simple Coulomb blockade theory since in this experiment only the conductance of dot 1 is directly being measured, and there is negligible tunneling probability between the second dot and the 2D reservoirs. One possible mechanism leading to the appearance of the peaks which reflect a change in the occupancy of dot 2 is inelastic cotunneling. Indeed, as will be further discussed in the following section, the appearance of these peaks associated with dot 2 in the measured conductance of dot 1 is evidence that the interdot interaction is not purely capacitive. The boundaries corresponding to an internal redistribution of charge in Fig. 3.5(a) are not present in the data because a conductance maximum requires a change in the total number of electrons $(N_1 + N_2)$.

Applying Eqn. (3.27) to the data of Fig. 4.12 to extract the value of the interdot capacitance assuming a purely capacitive interaction yields a value of $C_{dot1,dot2} \cong 60$ aF, which would represent approximately 20% of the total dot capacitance of 275 aF measured

in Sec. 4.3. In contrast, recent experiments [Crouch *et al.*, 1996] and calculations [Golden, 1995] predict an interdot capacitance of $C_{dot1,dot2} \cong 20$ aF for a coupled quantum dot system similar to the one studied here. The discrepancy results from neglecting the effects of finite interdot tunneling in the system.

As detailed in chapter 3, a more complete description of the coupled dot system requires consideration of charge fluctuations due to tunnel events between the dots in addition to purely capacitive interdot interaction. It was found in Chapter 3 that allowing electrons to be shared between the two dots lowers the ground state energy of the system and leads to a splitting F of adjacent columns in the charging diagram, as indicated in Fig. 4.12(b). Using Eqns. (3.30) and (3.32) for the predicted fractional splitting in the low interdot conductance limit, which is the case here with $G_{BE} \cong 0.32\ e^2/h$, including a constant geometrical interdot capacitance value of $C_{dot1,dot2} \cong 20$ aF as described above, we find a theoretically predicted value of $f_c = 0.17$. The experimentally observed splitting value F, as defined in Fig. 3.6, was measured for the 9 splitting points visible in the data of Fig. 4.12, and then normalized to the maximum value of F measured from the large interdot conductance data of Fig. 4.16(b). The average value is found to be $f_c = 0.16$, agreeing well with the predicted fractional splitting value.

Shown in Fig. 4.14 are conductance plots similar to Fig. 4.12, but with $V_B = V_E = -561$ mV, corresponding to an interdot tunnel conductance of 0.6 e^2/h. This represents approximately one-half mode of conductance connecting the two dots. The data in Fig. 4.15 are selected traces extracted from Fig. 4.14(a). As before, the data of Fig. 4.14 exhibit periodicities in each gate voltage direction. However, there are two marked differences when compared with the data of Fig. 4.12: 1) the secondary peaks have become more prominent, and 2) the splitting F between adjacent columns of unit cells has increased. In this regime of finite interdot tunneling, as described in Chapter 3, quantum charge fluctuations between the two dots dominate the interdot interaction, and N_1 and N_2

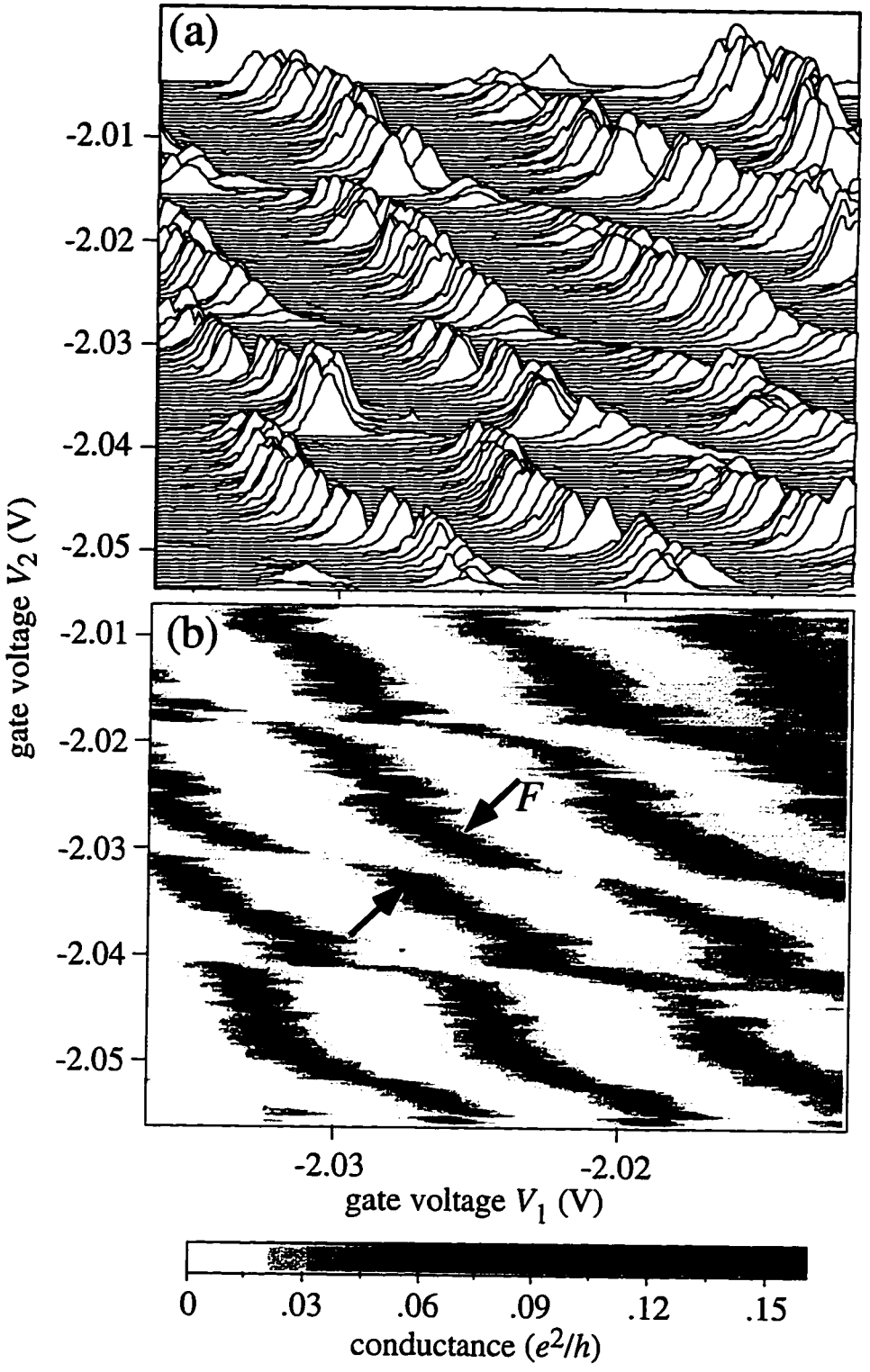


Fig. 4.14 (a) Conductance data for $G_{BE} \approx 0.6\ e^2/h$ as a function of the two side gate voltages V_1 and V_2. (b) Gray-scale representation of the same conductance data, showing the splitting F discussed in the text.

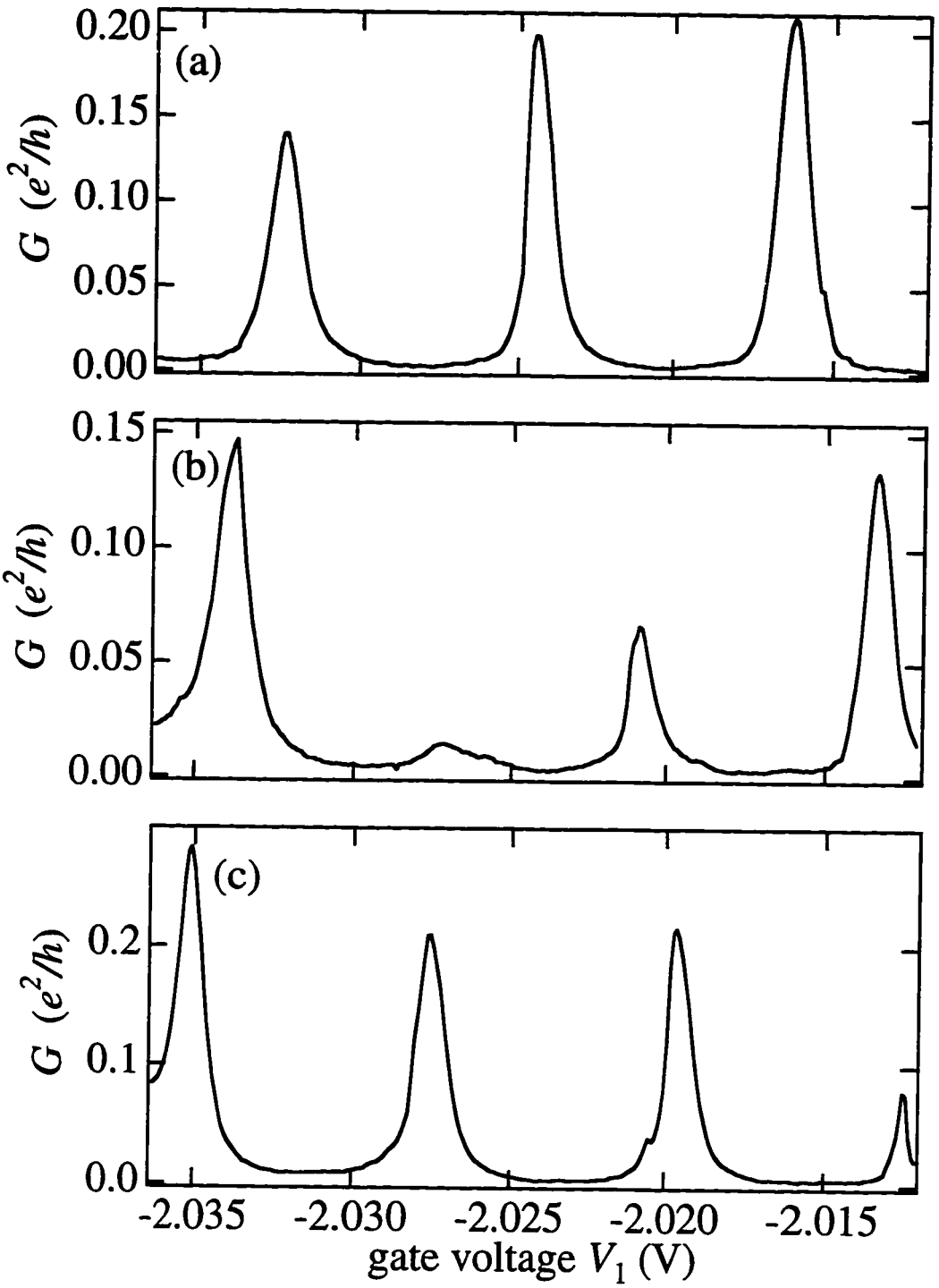


Fig. 4.15 Representative conductance traces extracted from Fig. 4.14 for V_2 = -2.046 V (a), V_2 = -2.032 V (b), and V_2 = -2.025 V (c).

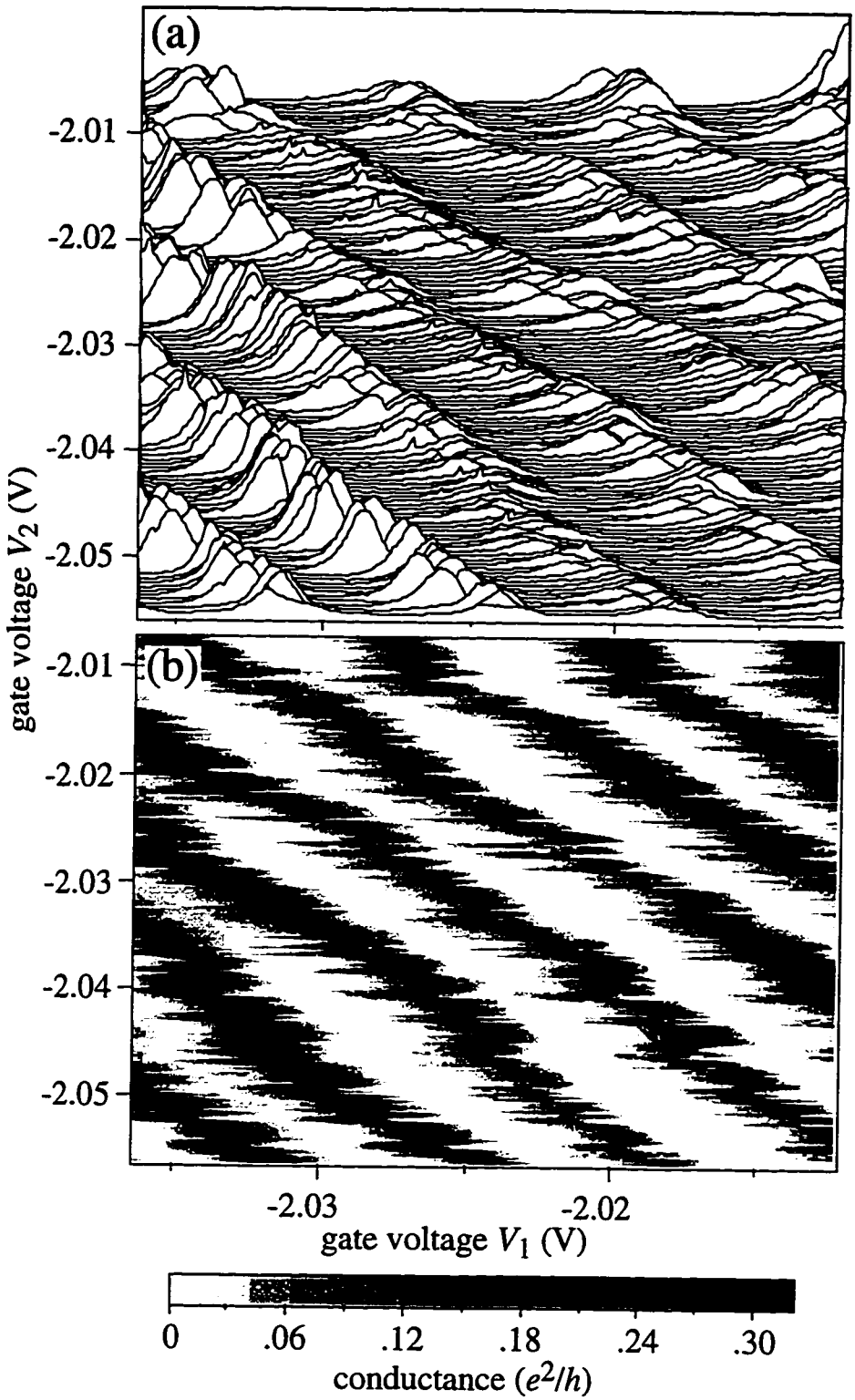


Fig. 4.16 (a) Conductance data for $G_{BE} \approx 1.9\ e^2/h$ as a function of the two side gate voltages V_1 and V_2. (b) Gray-scale representation of the same conductance data.

are no longer well-defined quantities. Comparing the data of Fig. 4.14 to the charging diagram of Fig. 3.6, which includes the role of interdot tunneling as described in Sec. 3.4.2, we can clearly identify the regions corresponding to different values of the total electron number $N_1 + N_2$. The fractional splitting f_c between adjacent columns in the data is measured for each splitting point seen in Fig. 4.14(b); the average value is $f_c = 0.43$. The increase in the magnitude of the secondary conductance maxima seen in Fig. 4.14 is also a result of increased quantum charge fluctuations between the dots, by which an electron on dot 1 can tunnel to dot 2; the behavior of these secondary peaks is discussed further later in this section.

Figures 4.16(a) and 4.16(b) show conductance data for the case where there is approximately one mode coupling the two dots, $G_{BE} \cong 1.9\ e^2/h$. In this strong coupling regime, the two dots are seen to behave essentially as a single large dot, with the total electron number $N_1 + N_2$ and the capacitance of the large dot to each of the gates determining the Coulomb blockade characteristics. The conductance pattern in Fig. 4.16(b) consists of alternating straight stripes of conductance maxima and minima and exhibits no jumps in peak positions which would indicate addition of an electron to one of the individual dots. Rather, the total electron number in the large dot can be tuned by each gate electrode separately. The onset of this behavior is predicted in the theory of [Golden and Halperin, 1996; Matveev *et al.*, 1996], who calculate that the coupled dot system should behave as a single large composite dot for interdot conductance of exactly $2e^2/h$. From the periodicities in each gate voltage direction we measure the capacitance of this large dot to each of the gates of $C_{dot,gate1} \cong 25$ aF and $C_{dot,gate2} = 27$ aF.

Figure 4.17 summarizes the experimentally determined relationship between the fractional splitting f_c and the interdot tunnel conductance G_{BE} together with the theoretically predicted form for weak and strong coupling from Eqns. (3.30), (3.31) and (3.32). Also shown is a possible interpolating function between the weak and strong

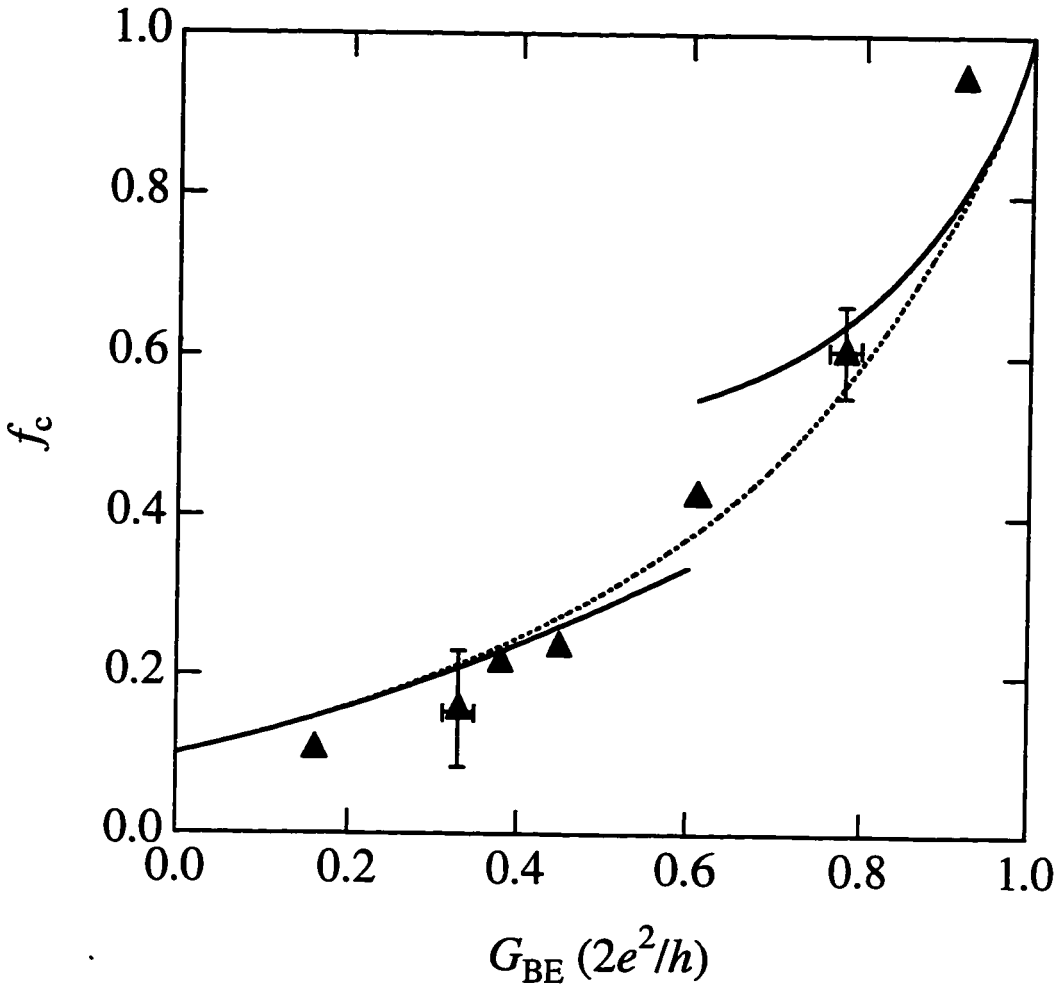


Fig. 4.17 Fractional splitting f_c plotted as a function of the interdot tunnel barrier conductance G_{BE}. Solid curves are theoretically predited forms for $f_c(G_{BE})$ from Eqn. (3.30) and (3.31) in the weak- and strong-tunneling limits. The dashed curve is a possible interpolating function. Triangles are experimentally measured splitting data. The theoretical form for f_c takes into account a constant interdot capacitance of 20 aF in accordance with Eqn. (3.32), with $C/(C + 2C_{int}) \approx 0.9$.

coupling limits [Golden and Halperin, 1996; Matveev *et al.*, 1996]. The plotted experimental data are determined by averaging over all the splitting points F (as defined in Fig. 4.12(b)) seen in a measurement of conductance as a function of V_1 and V_2 at a given value of G_{BE} and normalizing these values of F to the maximum splitting observed in Fig. 4.16(b) in order to obtain the fractional splitting value f_c. As predicted by the theory, the observed fractional splitting approaches unity at $G_{BE} \cong 2e^2/h$ in the strong tunneling limit, and approaches zero in the weak tunneling limit. The theory has no adjustable parameters except for the zero intercept which, as discussed in Sec. 3.4.2, is determined by the constant geometric interdot capacitance $C_{\text{dot 1,dot 2}} \approx 20$ aF.

Investigation of Secondary Peaks

This section describes a second series of experiments which were performed using the same device as in the previous section in order to further investigate the transport properties of the parallel coupled dot system. For this set of experiments, gates 1 and 2 are held at the same voltage and swept together, and the conductance through dot 1 is measured at various values of the interdot conductance G_{BE}, while dot 2 is set to be nonconducting. This corresponds to taking traces along the diagonal line $V_1 = V_2$ in the charging diagrams, as shown schematically in Fig. 4.18, directly intersecting the different boundaries of various charge configuration unit cells.

Figures 4.19 through 4.21 show the conductance G_1 of dot 1, measured using ohmic contacts I and II, as a function of the gate voltage on side gates 1 and 2, $V_1 = V_2$, at values of the interdot tunnel conductance between $G_{BE} \cong 0$ and $G_{BE} \cong 2e^2/h$. Shown in Fig. 4.22 and 4.23 are similar data taken during a different sample cooldown. In all of these traces, the quantum point contacts of dot 2 are set to $G_{BC} = G_{EF} = 0$, so that there

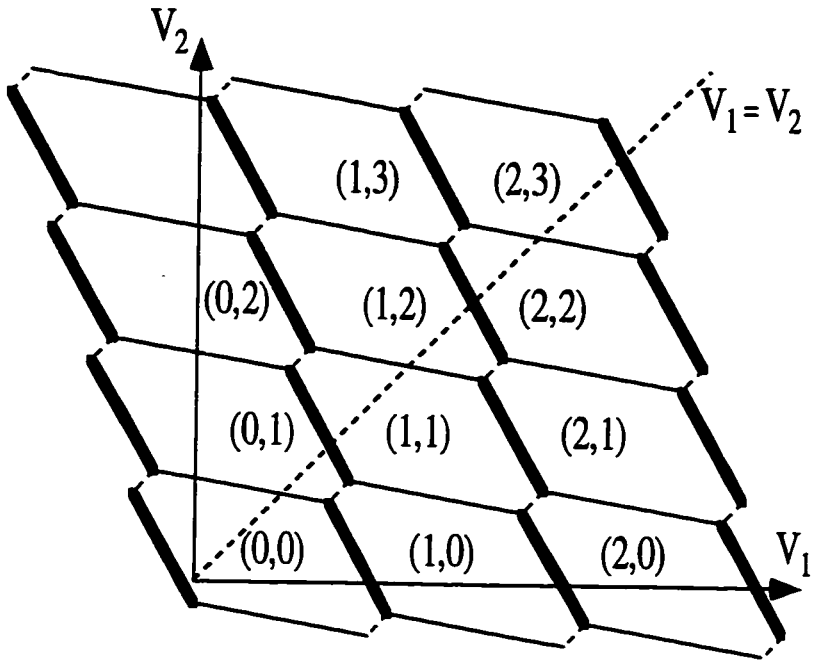


Fig. 4.18 Schematic charging diagram for coupled quantum dot system with no interdot tunnel conductance showing stable charge configurations (N_1, N_2), from Eqn. (3.22). The dotted line $V_1 = V_2$ indicates the different charge state boundaries which may be encountered when V_1 and V_2 are swept simultaneously. Primary peaks correspond to crossing boundaries where the occupancy of dot 1 changes, shown in bold. Secondary peaks are seen when a boundary corresponding to a change in the occupancy of dot 2 is crossed.

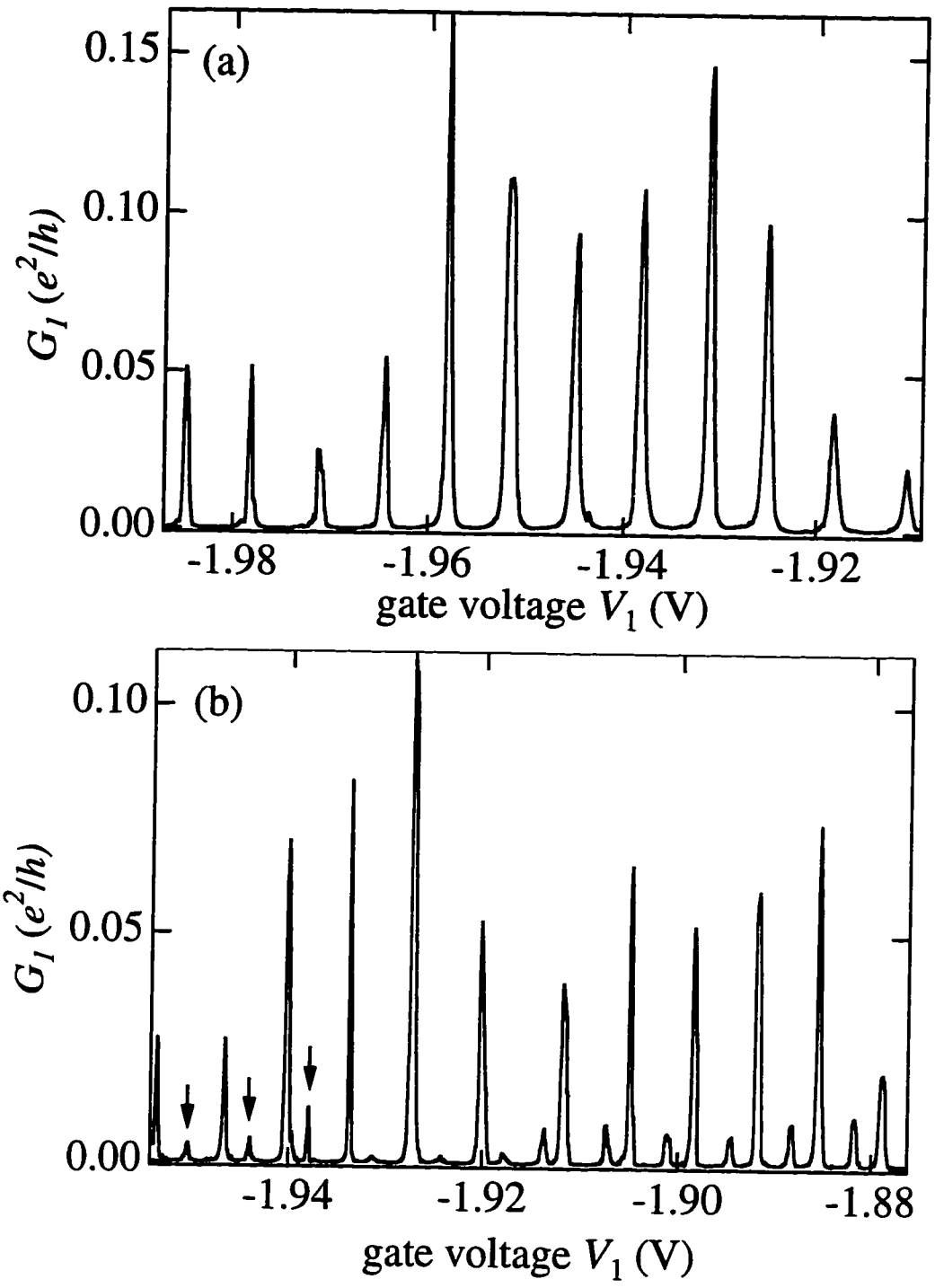


Fig. 4.19 Conductance G_1 of dot 1 measured as a function of the two side gate voltages $V_1 = V_2$ which are swept together, for (a) $G_{BE} = 0$, and (b) $G_{BE} \approx 0.8\ e^2/h$. The arrows in (b) indicate the first three secondary peaks.

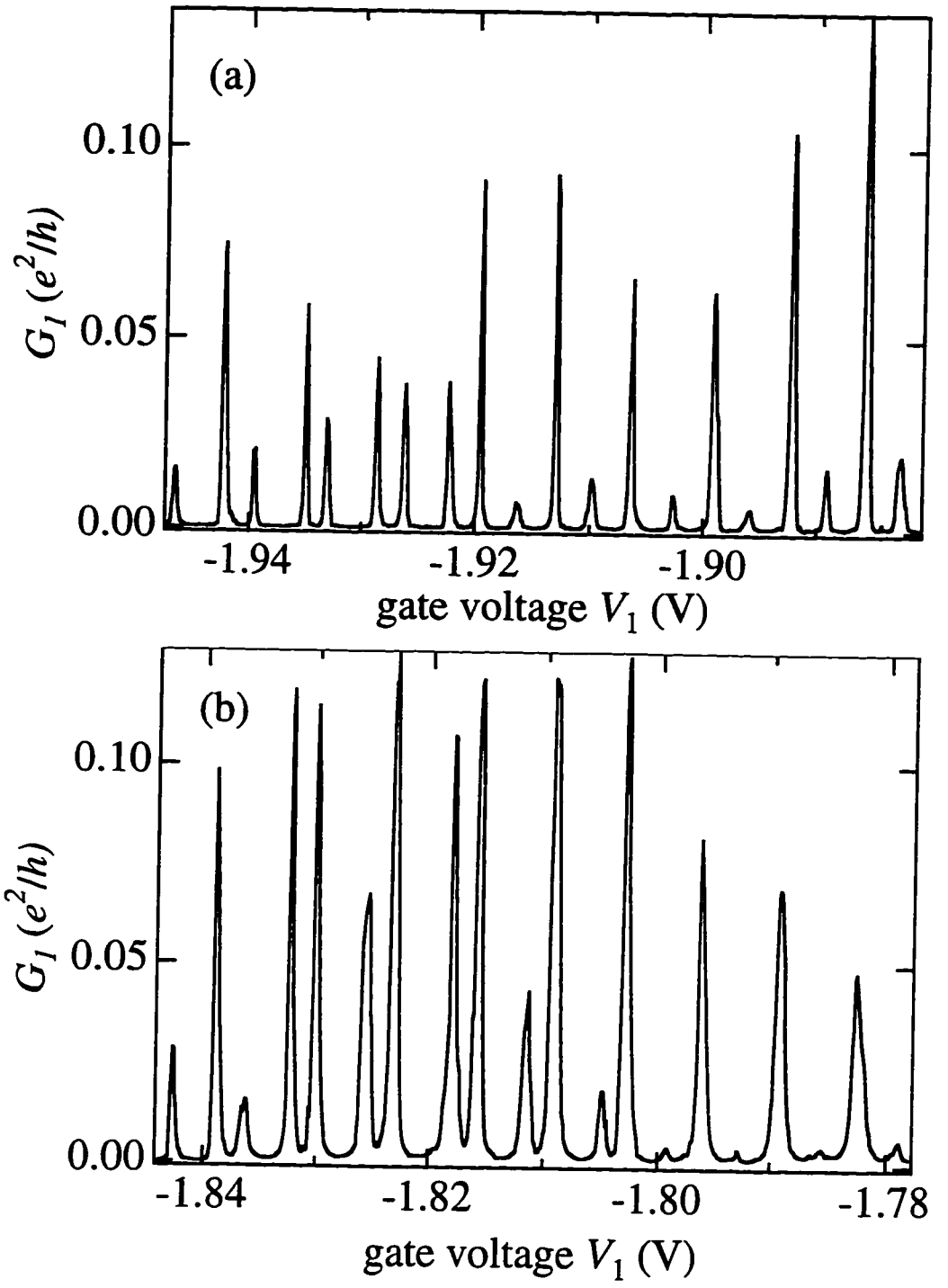


Fig. 4.20 Conductance G_1 of dot 1 measured as a function of the two side gate voltages $V_1 = V_2$ for (a) $G_{BF} \approx 1.0\ e^2/h$, and (b) $G_{BF} \approx 1.2\ e^2/h$.

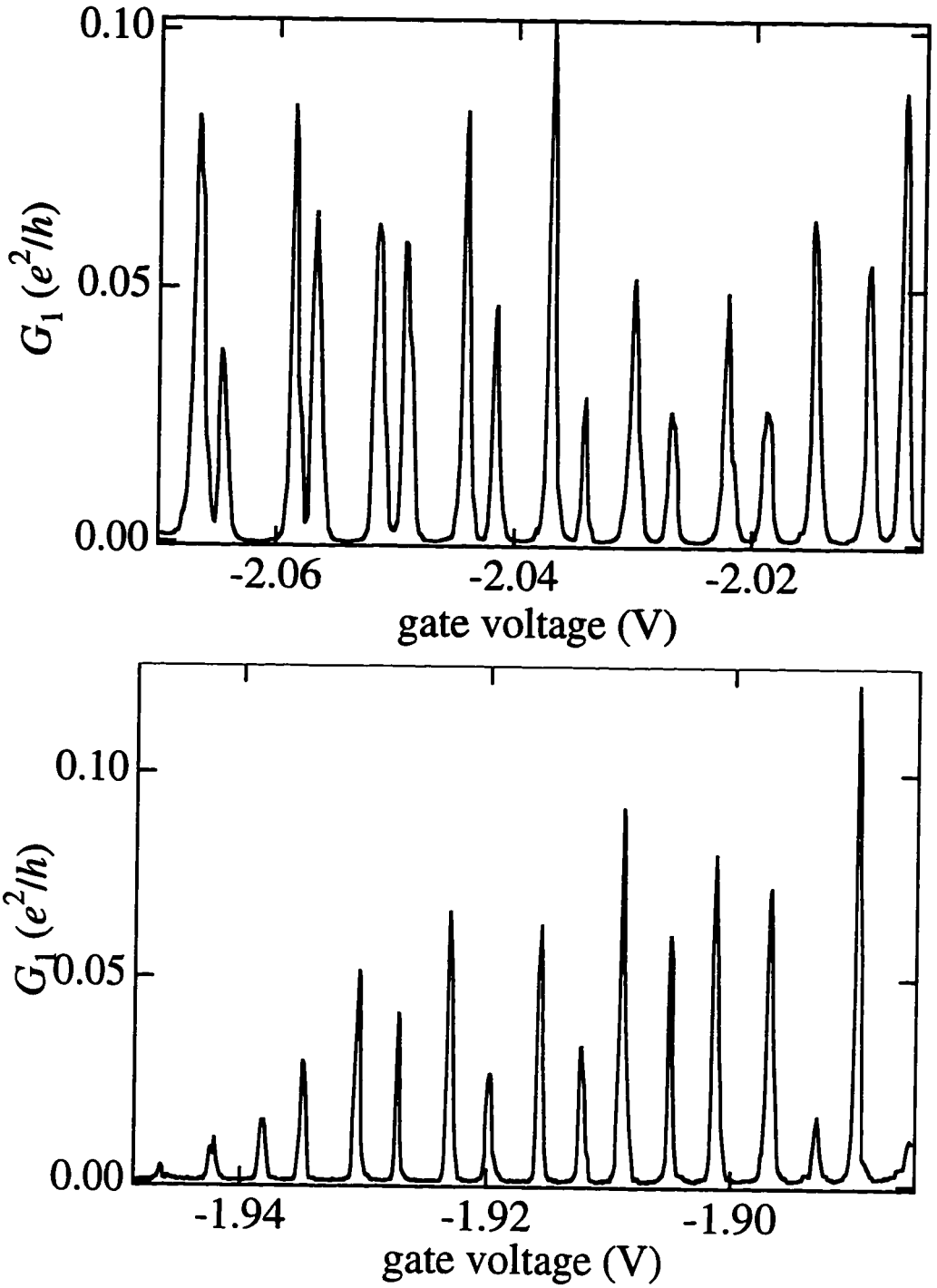


Fig. 4.21 Conductance G_1 of dot 1 measured as a function of the two side gate voltages $V_1 = V_2$ for (a) $G_{BF} \approx 1.6\ e^2/h$, and (b) $G_{BF} \approx 1.9\ e^2/h$.

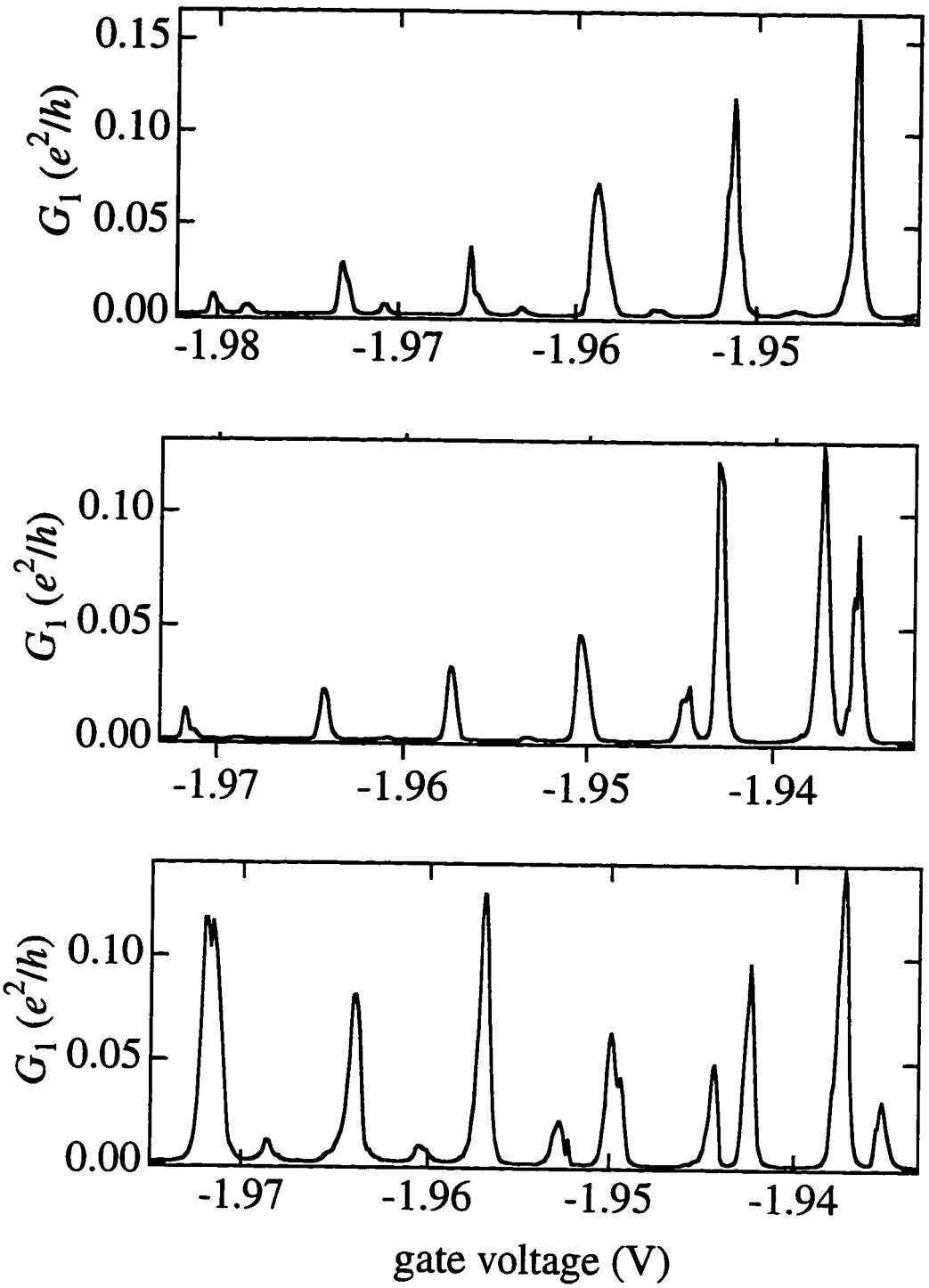


Fig. 4.22 Conductance G_1 of dot 1 measured as a function of the two side gate voltages $V_1 = V_2$ for (a) $G_{BE} \approx 0.2\ e^2/h$, and (b) $G_{BE} \approx 0.5\ e^2/h$, and (c) $G_{BE} \approx 0.9\ e^2/h$.

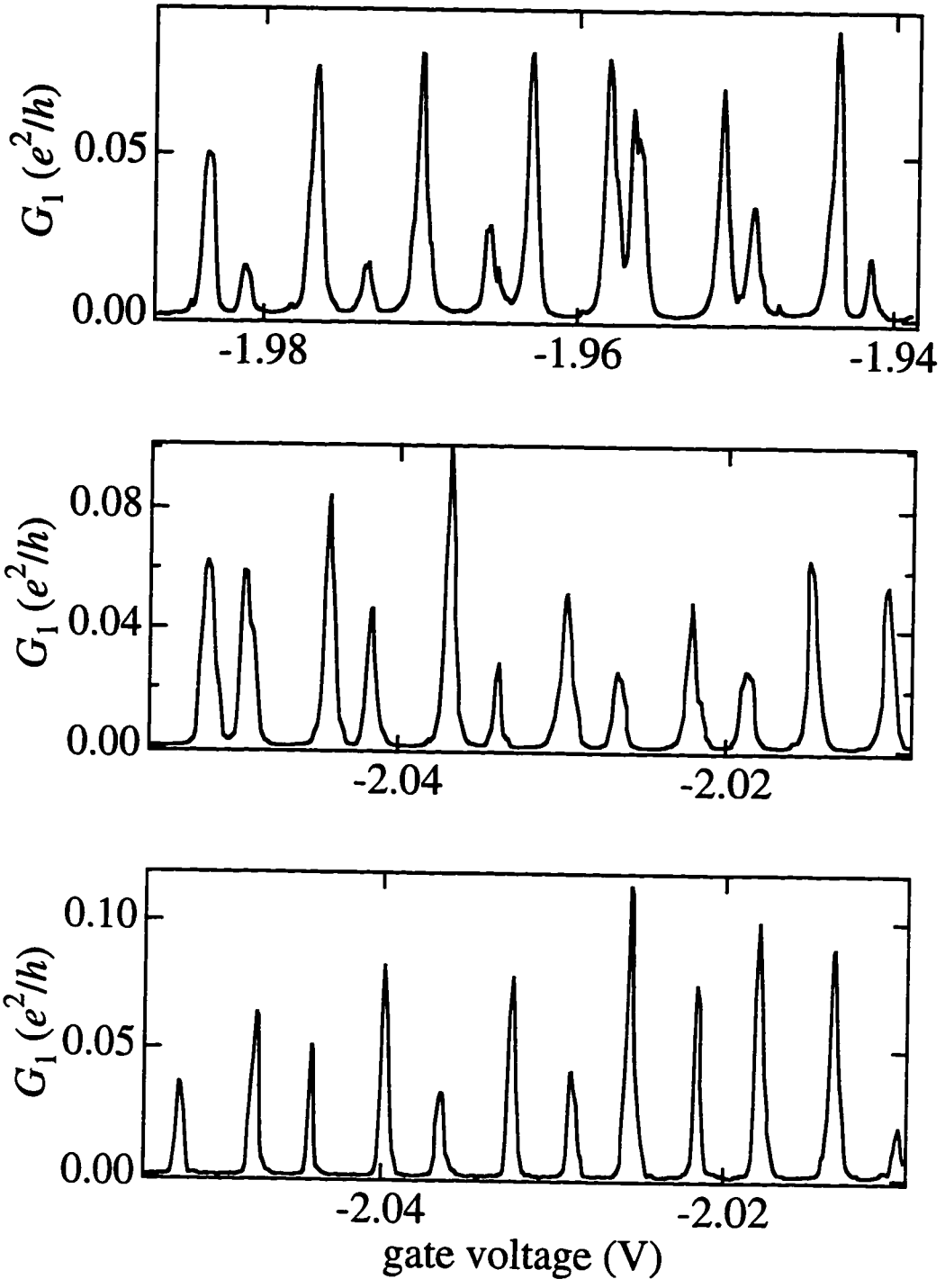


Fig. 4.23 Conductance G_1 of dot 1 measured as a function of the two side gate voltages $V_1 = V_2$ for (a) $G_{BE} \approx 1.2\ e^2/h$, and (b) $G_{BE} \approx 1.6\ e^2/h$, and (c) $G_{BE} \approx 1.9\ e^2/h$.

is negligible tunneling probability between dot 2 and the 2D reservoirs, and dot 2 is nonconducting. As described in the previous section, the interdot tunnel conductance G_{BE} is inferred from the gate voltages $V_B = V_E$ by accounting for the influence of the adjacent electrostatic gates.

We will first focus on the data shown in Figs. 4.19 through 4.21. Figure 4.19(a) shows the conductance G_1 of dot 1 for the case of zero interdot tunnel conductance, $G_{BE} = 0$, as a function of the voltage on side gates 1 and 2 which are held at the same potential. Evenly spaced Coulomb blockade conductance peaks as a function of gate voltage are seen with a period $\Delta V_g \approx 6.7$ mV, corresponding to a capacitance between dot 1 and both gates 1 and 2 of $C_{dot1,gates1+2} \approx 24$ aF. The most striking feature of the conductance traces taken at finite interdot tunnel conductance, shown in Figs. 4.19(b), Figs. 4.20 (a) and (b), and Fig. 4.21(a), is the emergence of a set of secondary peaks amidst the primary Coulomb blockade peaks of Fig. 4.19(a). These secondary peaks grow in amplitude relative to the primary peaks, and their positions shift, until $G_{BE} \cong 2e^2/h$. With approximately one mode between the dots, shown in Fig. 4.21(b), the double dot system behaves as a single large composite dot exhibiting regularly spaced Coulomb blockade peaks with a period approximately half that for the single, well isolated dot of Fig. 4.19(a). From the period of $\Delta V_g \approx 3.6$ mV for the data of Fig. 4.21(b), we calculate a capacitance between the large composite dot and the two swept side gates of $C_{large\ dot,gates1+2} \approx 44$ aF which as expected is approximately twice the value of $C_{dot1,gates1+2} \approx 24$ aF calculated above for a single well-isolated dot.

As illustrated graphically in Fig. 4.18, the secondary peaks observed in the conductance of dot 1 reflect changes in the stable charge configuration of the coupled dot system. As done in the previous section, we will begin the analysis of the results for the limit of weak interdot tunneling by invoking the capacitive charging model of Fig. 3.4 which neglects interdot tunneling. In the limit of weak interdot tunnel coupling of Fig. 4.19(b), comparing

the data to the capacitive charging diagram of Fig. 3.5 indicates that a secondary peak results from crossing a charge state unit cell boundary in which the charge of dot 2, the nonconducting dot, changes by one electron. This picture also provides a qualitative explanation of the occasional occurrence of two adjacent primary peaks. These adjacent primary peaks correspond to regions in gate voltage in which the stable electron configuration of the system is such that there is a charge difference of two electrons between the dots. A detailed comparison of both primary and secondary peak positions with theory is difficult, as this requires knowledge of the exact capacitances in the system and a precise value for the interdot tunneling conductance.

Figure 4.24 demonstrates the strong correlation between the interdot conductance and the secondary peak amplitudes. Figure 4.24(a) plots the ratio of the amplitude of the secondary peaks, A_s, to that of the primary peaks, A_p, at various values of the voltage $V_B = V_E$ on the inner quantum point contact gates. The amplitudes are measured as shown in Fig. 4.24(b), and the ratio A_s/A_p refers to the average, taken over all the peaks in a given trace, of the amplitude ratio of each pair of secondary peak and its neighboring primary peak. Also shown in the solid line in Fig. 4.24(a) is the measured conductance curve of the inner quantum point contact G_{BE} as a function of gate voltage, offset by 175 mV to account for the influence of the other gates, as described in Sec. 4.5.1. The close correlation between these data sets is evidence that the origin of the secondary peaks lies in tunneling of electrons between the two dots; this will be further explored in the next section. The ratio A_s/A_p approaches unity as the interdot conductance G_{BE} approaches $2e^2/h$, providing further evidence for the theoretical predictions [Golden and Halperin, 1996; Matveev *et al.*, 1996] that at one mode of conductance connecting the two dots the double dot system behaves as a single composite dot.

We now turn to developing an understanding of the origin of these secondary peaks which appear in the measured conductance G_1 of dot 1. At low interdot tunnel

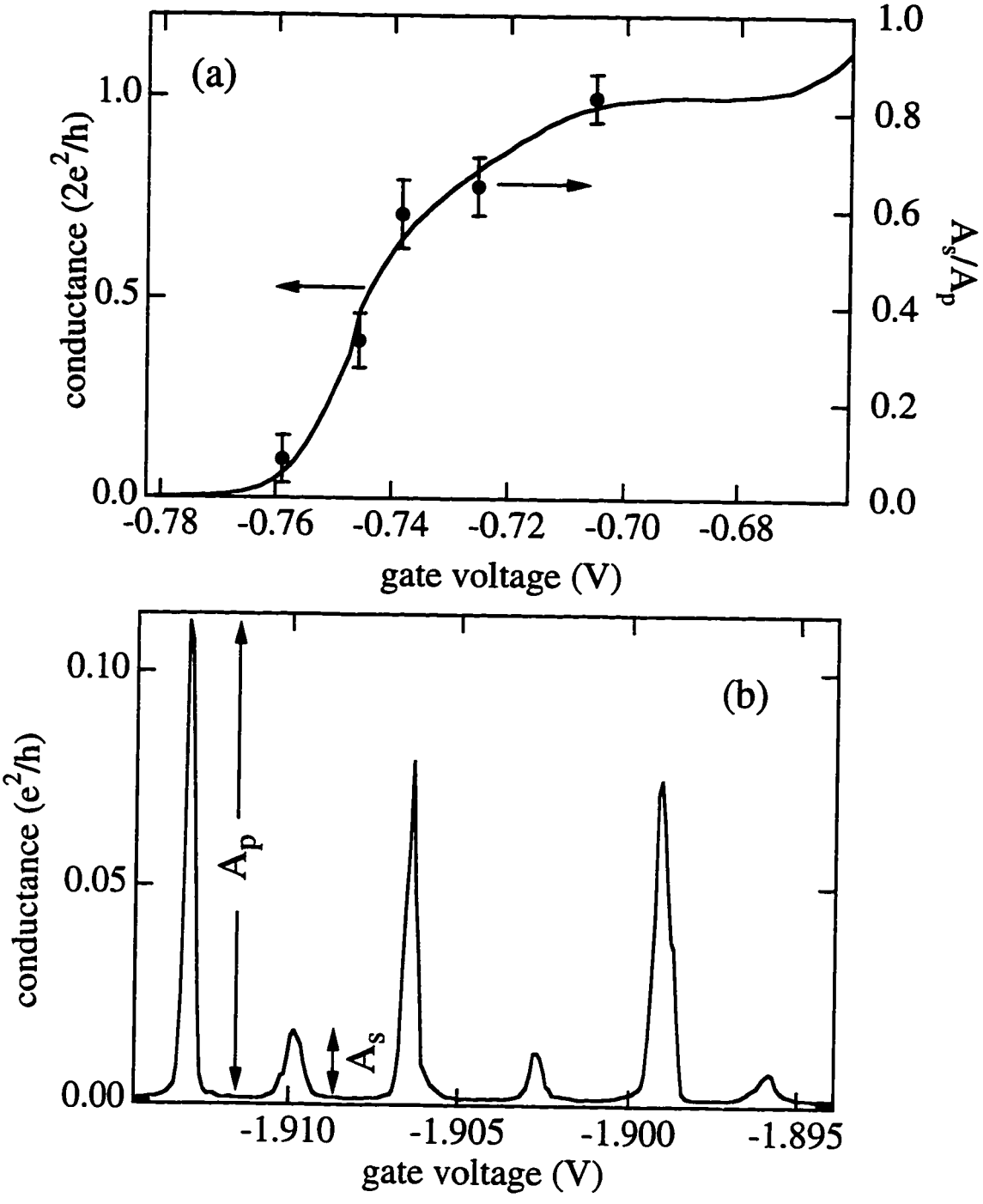


Fig. 4.24 (a) Measured inter-dot barrier conductance G_{BE} as a function of gate voltage $V_B = V_E$ (left scale). Shown as filled circles are the secondary to primary peak amplitude ratios A_s/A_p at various values of $V_B = V_E$, averaged over at least 10 peak pairs, illustrating the correlation with G_{BE}. (b) A typical conductance trace defining the amplitudes A_s and A_p.

conductance, one possible mechanism leading to the appearance of the peaks which reflect a change in the occupancy of dot 2 is inelastic cotunneling, a higher-order correlated tunneling process [Averin and Nazarov, 1990; Matveev *et al.*, 1996]. Cotunneling is a virtual process which does not require energy conservation in the dot. The way in which this process can lead to the secondary conductance peaks is shown schematically in Fig. 4.25. In this process, when the Coulomb blockade is lifted on dot 2 but not on dot 1, an electron tunnels from dot 1 to dot 2, and then another electron tunnels from the source reservoir of dot 1 onto dot 1. In this way, after the cotunneling process is completed, dot 1 is returned to the state with no extra charge while the occupancy of dot 2 has increased by one electron. A similar process by which the extra electron on dot 2 tunnels onto dot 1, while an electron on dot 1 simultaneously tunnels to the drain reservoir returns the coupled dot system to its original state, but with the net result that one electron has been transferred from the source to the drain of dot 1 and is measured as a finite conductance peak in G_1.

Recently, the temperature dependence of such inelastic cotunneling conductance processes has been calculated for a coupled dot system. In the limit of low interdot tunnel conductance $G_{\text{interdot}} << e^2/h$ Matveev et al. [Averin and Nazarov, 1990; Matveev *et al.*, 1996] predict a quadratic temperature dependence of the cotunneling secondary peak maxima

$$G_{\max} \sim G_{AB} G_{BE} T^2. \tag{4.3}$$

The suppression of current through the system is caused by a vanishing overlap between the two ground states, before and after a tunneling event, as the temperature is lowered. For the limit of strong tunneling between the dots, the temperature dependence of the cotunneling peaks is also predicted to exhibit an algebraic dependence on temperature, with $G_{\max} \sim T^{1/4}$.

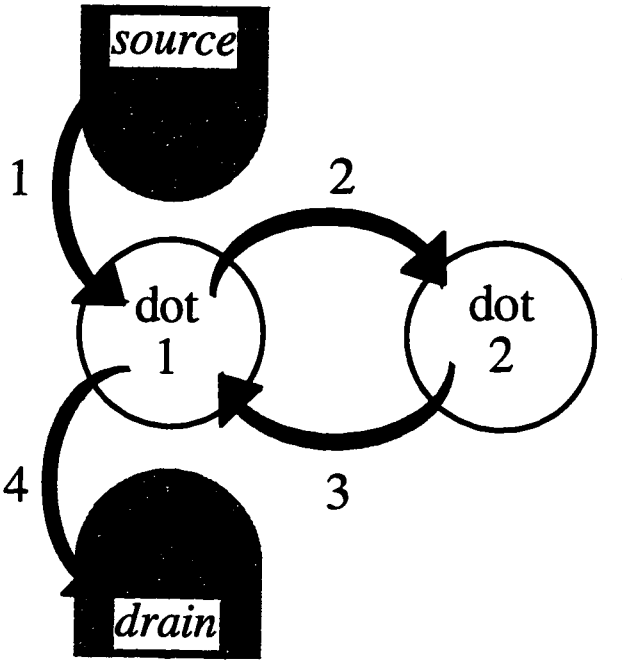


Fig. 4.25 Schematic of inelastic cotunneling process which gives rise to secondary conductance peaks discussed in the text. With the Coulomb blockade on dot 2 lifted, an electron tunnels from the source to dot 1 (1) while simultaneously an electron tunnels from dot 1 to dot 2 (2), satisfying the charge degeneracy condition on dot 2. The extra electron on dot 2 can then tunnel back to dot 1 (3) while an electron from dot 1 tunnels out to the drain (4), resulting in a net nonzero measured current through dot 1.

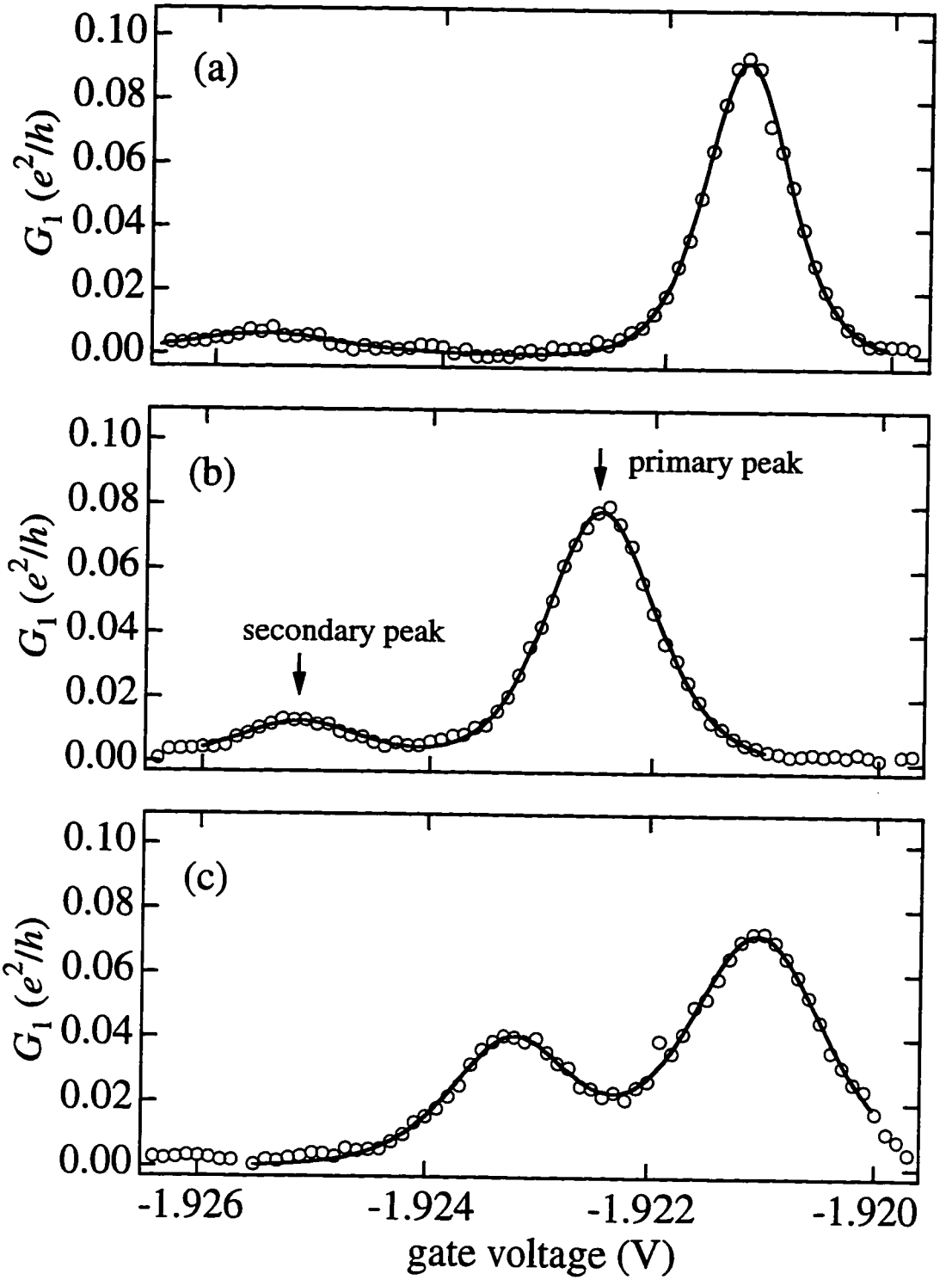


Fig. 4.26 Measured conductance G_1 (open circles) of dot 1 as a function of voltage on the two side gates $V_B = V_E$ with $G_{BE} \approx 0.8\ e^2/h$ showing a primary and secondary peak pair at (a) T_{mc} = 190 mK, (b) T_{mc} = 250 mK, (c) T_{mc} = 300 mK. Solid lines are fits to thermally broadened lineshapes discussed in the text.

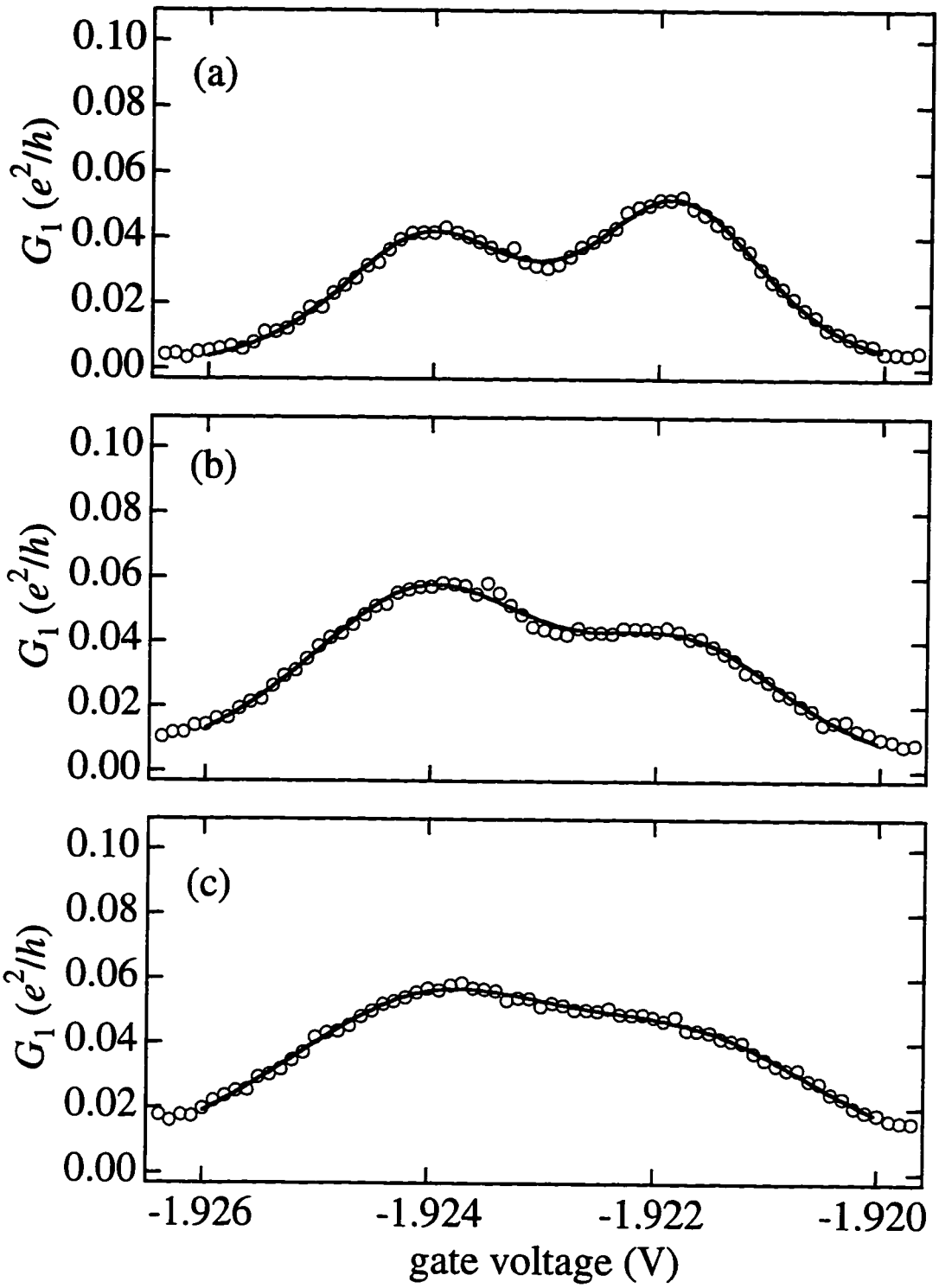


Fig. 4.27 Measured conductance G_1 (open circles) of dot 1 as a function of voltage on the two side gates $V_B = V_E$ with $G_{BE} \approx 0.8\ e^2/h$ showing the primary and secondary peak pair from Fig. 4.26 at (a) $T_{mc} = 400$ mK, (b) $T_{mc} = 500$ mK, (c) $T_{mc} = 600$ mK. Solid lines are fits to thermally broadened lineshapes discussed in the text.

Figures 4.26 and 4.27 illustrate the evolution of a primary and secondary peak pair with temperature, taken at an interdot conductance value of $G_{BE} \approx 0.4\ e^2/h$. The open circles in the figures are the data, and the solid lines are fits of the data to a function which is the sum of two thermally broadened lineshapes of Eqn. (3.19). It is seen that a thermally broadened lineshape fits both primary and secondary peaks well at all measured temperatures. A marked difference in the behavior of the pair of conductance peaks is the difference in the temperature dependence of the primary and secondary peaks. The primary peaks are seen to decrease in amplitude with increasing temperature, while the secondary peaks increase in amplitude.

We now turn to analyzing these primary and secondary conductance peak heights as a function of the temperature, and compare them to the theoretical predictions of Matveev *et al.* [1996]. Figure 4.28(a) plots on a double logarithmic scale the temperature dependence of the amplitudes of both secondary and primary peaks shown in Figs. 4.26 and 4.27. According to Eqn. (3.19) the primary Coulomb blockade peaks are expected to follow a T^{-1} power law in this temperature range of $T < \Delta E/k_B \approx 50\ \mu eV/\ k_B \approx 600$ mK, and the dotted line in Fig. 4.28(a) is a fit to this temperature dependence. The dashed line in Fig. 4.28(a) is a fit of the secondary peak amplitudes to a $G_{peak} \sim T^2$ dependence, as predicted by Matveev *et al.* [1996] in the $G_{interdot} << e^2/h$ regime. While the data in Fig. 4.28(a) is for $G_{interdot} \approx 0.4\ e^2/h$, we see that the quadratic temperature dependence is not the best fit over the entire temperature range. The higher temperature secondary peak maxima data points exhibit a decreased slope compared to the lower temperature data.

Fig. 4.28(b) plots the evolution with mixing chamber temperature T_{mc} of the electron temperature T_e as calculated from the full-width at half-maximum (FWHM) of both primary and secondary peaks. We use the relation from Eqn. (3.19b), $\Delta V_{FWHM} = (3.5k_BT/e)(C/C_g)$, with the total dot capacitance C = 320 aF and the gate capacitance C_g = 23 aF from the measured values for each dot. For the primary Coulomb blockade peaks

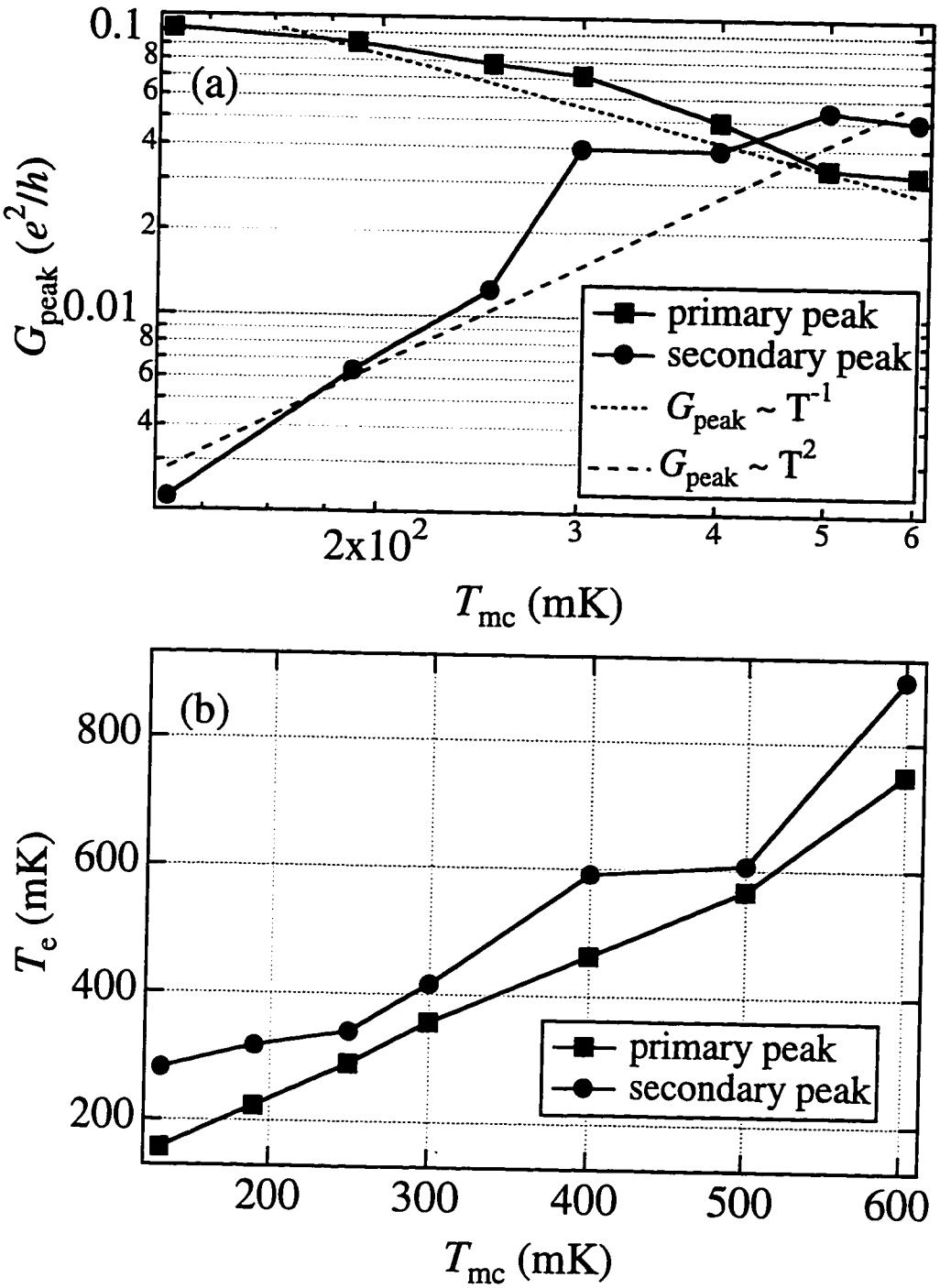


Fig. 4.28 (a) Temperature dependence of peak heights for the primary and secondary peaks of Figs. 4.26 and 4.27. (b) Relationship between mixing chamber temperature T_{mc} and electron temperature T_e calculated from full-width at half-maximum of thermally broadened lineshape fits, for the same primary and secondary peak pair as in (a).

a linear temperature dependence is observed over the entire temperature range, as predicted by Eqn. (3.19b). The calculated electron temperatures for the secondary peaks also exhibit an approximately linear temperature dependence, but with a consistently larger value relative to the primary peak resonances. For both peaks it is seen that the calculated electron temperature is somewhat higher than the nominal mixing chamber temperature, which can be interpreted as resulting from a broadening of the peaks by residual rf noise [Kemerink and Molenkamp, 1994] or a broadening of levels by the fluctuations of the dot potential caused by electron trapping close to the dot [Field *et al.*, 1993; Cobden *et al.*, 1991].

4.5.2 Measurements with both dots conducting

Another set of experiments performed on the parallel double dot device of Fig. 4.1 involves simultaneous measurement of the conductance through both dots. In these experiments, we set the outer point contacts of dot 2 as well as dot 1 to be conducting, $G_{AB}, G_{BC}, G_{EF}, G_{DE} \approx .02\ e^2/h$, and use two separate measurement circuits to measure the conductance through dot 1 (using ohmic contacts I and II) and dot 2 (using ohmic contacts III and IV) simultaneously. As in the previous section, the two side gates are tied together so that $V_1 = V_2$, and the conductance is measured as a function of the voltage on these side gates. Figure 4.29 plots the simultaneously measured conductances G_1 and G_2 of dots 1 and 2 as a function of $V_1 = V_2$ for various values of the interdot conductance G_{BE}. As discussed earlier, G_{BE} is estimated by taking into account the influence of the other electrostatic gates of the device on the interdot barrier.

For the regime where approximately one mode of conductance connects the dots shown in Fig. 4.29(c), $G_{BE} \approx 2e^2/h$, we see that the Coulomb blockade oscillations in both G_1 and G_2 are in phase and have the same period. This is expected, since with one full mode

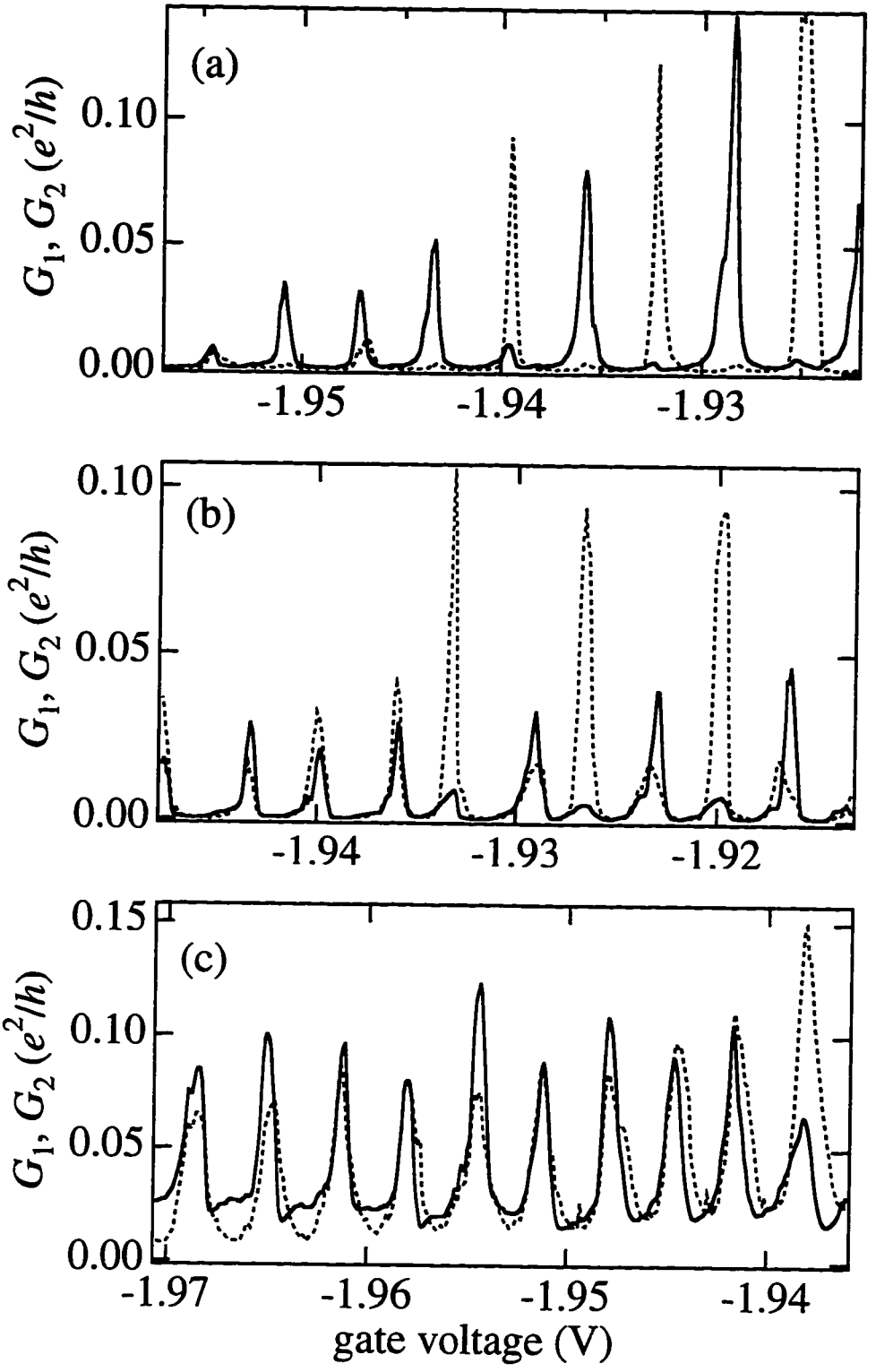


Fig. 4.29 Simultaneously measured conductances G_1 of dot 1 (solid line) and G_2 of dot 2 (dashed line) as a function of gate voltage $V_1 = V_2$ for (a) $G_{BF} \approx 0.2\ e^2/h$, (b) $G_{BF} \approx 1.1\ e^2/h$, and (c) $G_{BF} \approx 1.9\ e^2/h$.

connecting the two dots the double dot system behaves as a large composite dot. From the period of the conductance oscillations we calculate a capacitance between the two gates being swept (gates 1 and 2) and the large dot of 48 aF, which as expected is approximately twice the value of the capacitance between a single gate and the large composite dot measured in Sec. 4.5.1.

Shown in Fig. 4.29(a) and (b) are the conductances G_1 and G_2 of both dots as a function of the voltage on the side gates for a value of interdot conductance $G_{BE} \approx 0.2e^2/h$ for Fig. 4.29(a) and $G_{BE} \approx 1.1e^2/h$ for Fig. 4.29(b). As described in the previous section, with less than one mode of interdot tunnel conductance, a secondary peak structure becomes observable in the conductance traces of each dot. Significantly, it is seen that the larger amplitude primary Coulomb blockade peaks of one dot coincide with the secondary peaks observed on the neighboring dot, and vice versa. This constitutes direct evidence that the secondary peaks observed on one dot correspond to changes in the charge state of the neighboring dot, which are reflected in a primary Coulomb blockade peak observed on that neighboring dot. For a larger interdot tunnel conductance of $G_{BE} \approx 1.1e^2/h$ as in Fig. 4.29(b), we see that as in the previous section the amplitudes of the secondary peaks have grown relative to the primary peak amplitudes, and again the secondary peaks on one conductance trace correspond to the primary peaks measured in the conductance of the other dot.

Figure 4.30 is a plot of G_1 and G_2 at $G_{BE} \approx 0.9e^2/h$ illustrating a range in gate voltage in which the primary peaks and secondary peaks of both dots are seen to trade positions. This region of gate voltage likely corresponds to a point in which the charge difference between the two dots, in the picture of noninteracting dots, becomes two electrons. In this case, the alternating primary peak/secondary peak structure is interrupted by two adjacent primary peaks, as seen in Fig. 4.30 at V_g = -1.795 V. On either side of that point in gate voltage, the amplitudes of the primary and secondary peaks are seen to

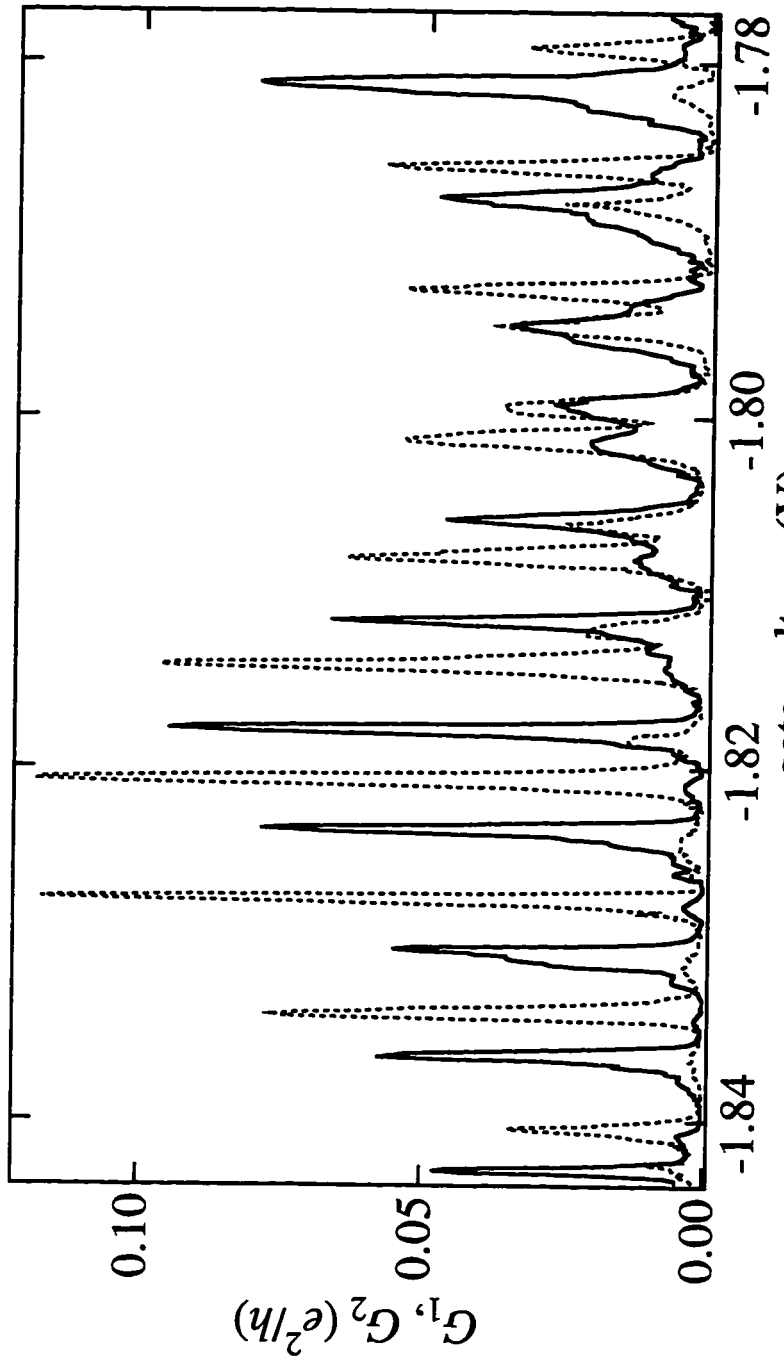


Fig. 4.30 Simultaneously measured conductances G_1 of dot 1 (solid line) and G_2 of dot 2 (dashed line) as a function of gate voltage $V_1 = V_2$ for $G_{BE} \approx 0.9\ e^2/h$, exhibiting an interchange of positions of primary and secondary conductance peaks.

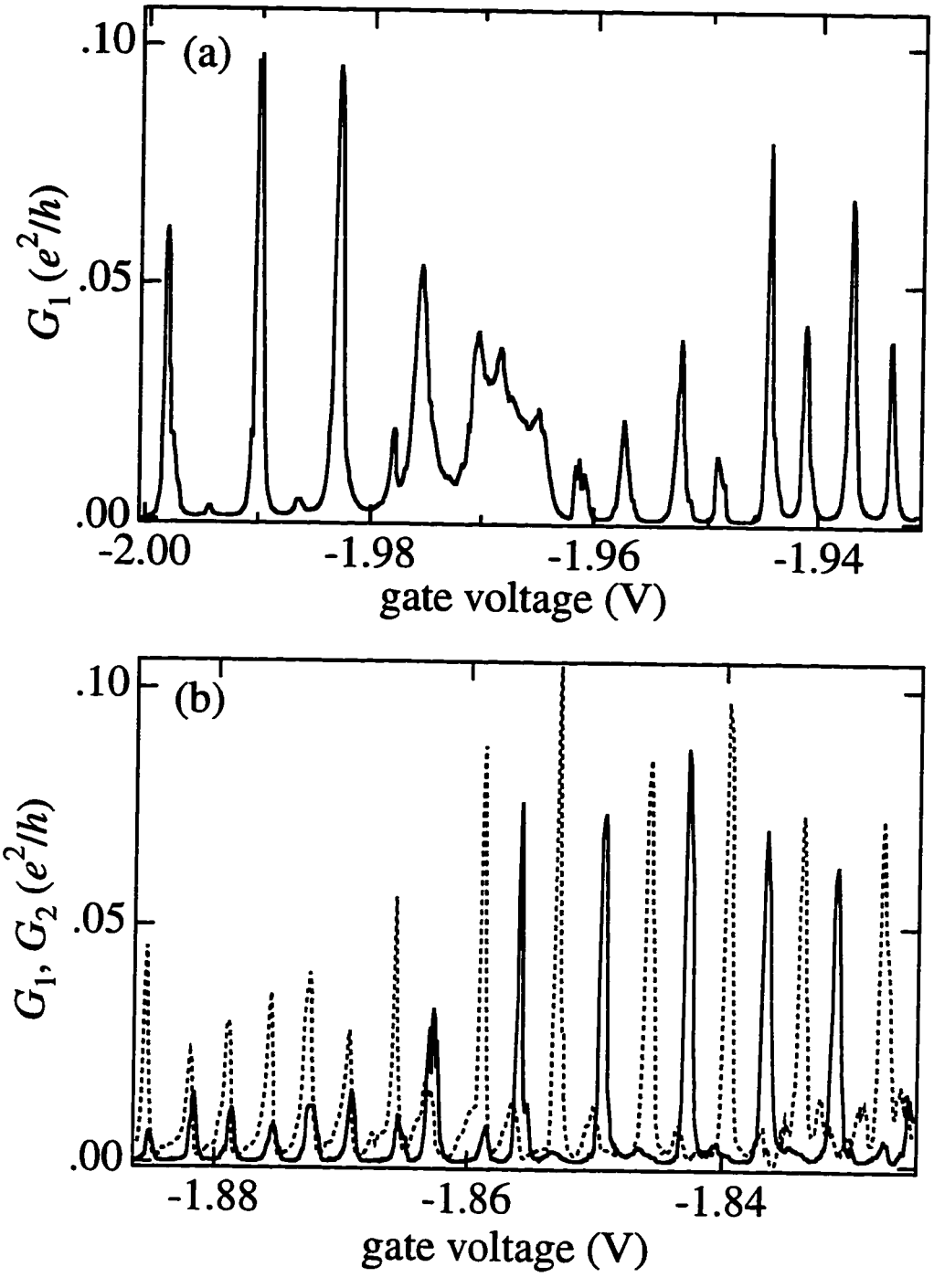


Fig. 4.31 (a) Conductance G_1 of dot 1 as a function of gate voltage $V_1 = V_2$ exhibiting an abrupt transition from one interdot conductance regime to another, as discussed in the text. (b) Simultaneously measured conductances G_1 of dot 1 (solid line) and G_2 of dot 2 (dashed line) as a function of gate voltage showing a similar phenomena.

become comparable as the lineshapes of each increasingly overlap.

Figure 4.31(b) is a plot of G_1 and G_2 as a function of $V_1 = V_2$ which exhibits a phenomena not expected from the simple coupled dot charging theory presented thus far. An abrupt transition region is observed at $V_1 = V_2 \approx -1.863$ V between regions in gate voltage exhibiting two distinct peak periodicities. For $V_1 = V_2 > -1.863$ V both primary and secondary peaks are seen in G_1 and G_2, with the primary conductance peaks of one dot corresponding to secondary peaks of the other dot. The conductance characteristics in this range of gate voltage resemble the data seen in Fig. 4.29(a) for $G_{BE} \approx 0.2e^2/h$. For $V_1 = V_2 < -1.863$ V however, the conductance peak structure of both dots exhibits a single periodicity of approximately half that of the primary peak period in the regime of $V_1 = V_2 > -1.863$ V, and there are no secondary peaks seen. In this range of gate voltage, the coupled dot system is seen to behave as a single large composite dot. This behavior resembles that seen in Fig. 4.29(c), where there is approximately one full mode connecting the two quantum dots. The transition region is seen to be very abrupt compared to the voltage scale of the peak periods, occurring over less than 3 mV. This phenomena is reproducible and independent of gate voltage sweep direction. Shown in Fig. 4.31(a) is a similar phenomenon observed in the measured conductance G_1 of dot 1 while G_2 was set to be zero by adjusting $G_{BC} = G_{EF} = 0$, with $G_{BE} \approx 0.8e^2/h$. The data in this figure were taken on a different day than those of Fig. 4.31(b). Similar to Fig. 4.31(b), there are two distinct regions of behavior separated by an abrupt transition region occurring at $V_g \approx -1.97$ V. However in this case it is for $V_g > -1.97$ V that the system behaves as a single large dot, while for $V_g < -1.97$ V we recover the alternating primary and secondary peak features characteristic of the parallel dot system with less than one mode of conductance between the dots.

A possible explanation for these observations may lie in the properties of the inner quantum point contact whose conductance G_{BE} determines the interdot tunnel coupling.

As was seen in the quantum point contact conductance traces of Fig. 4.2(a), apart from the conductance steps some of the conductance data exhibit additional structure as a function of gate voltage, likely due to electron backscattering in the constriction or resonant tunneling through impurity atoms in the channel. These additional features can lead to a non-monotonic change in conductance for a given change in gate voltage, such as those seen in Fig. 4.2 (a) for G_{AB}. Although the conductance G_{BE} of the inner point contact does not seem to exhibit any such irregularities in Fig. 4.2(b), the influence of the adjacent gates of the device likely alters the potential of the constriction formed by gates B and E and may introduce additional conductance structure not seen in a separate measurement of G_{BE}. It is plausible that upon sweeping the voltage on gates 1 and 2, as is done to obtain the conductance data of Fig. 4.31(a) and (b), the influence of these gates on the inner quantum point contact conductance G_{BE} may be such that G_{BE} changes non-monotonically, resulting in an abrupt change in the interdot tunnel conductance leading conductance, reflected in the data of Fig. 4.31.

An alternative explanation of the features shown in Fig. 4.31 involves the charging of electron trapping defects near the coupled quantum dot system. Such electron trapping events would shift the electrical potential of the interdot conductance channel relative to the Fermi level, resulting in abrupt changes in the value of the interdot tunnel conductance [Timp *et al.*, 1990]. As the voltages on gates 1 and 2 are varied, these defects may change their mean occupancy and give rise to the reproducible structures exhibited in Fig. 4.31.

CHAPTER V

Fabrication of Integrated Josephson Junction and Semiconductor Nanostructure Circuits

5.1 Introduction

Recently there has been much theoretical and experimental interest in the effects of a high-frequency potential $V_{ac}\cos(2\pi ft)$ on electron transport through small capacitance mesoscopic structures [Flensberg, 1992; Likharev 1994; Hadicke 1994; Bruder 1994; Hu 1993; Kouwenhoven 1994]. Investigations in the regime of $hf >> k_B T$ are expected to yield a multitude of new quantum phenomena. For example, recent experiments on semiconductor quantum dots in the Coulomb blockade regime in the presence of high-frequency (f ~ 20 to 30 GHz) time dependent potentials have demonstrated photon-assisted tunneling where the discrete photon energy becomes observable [Kouwenhoven 1994]. Other time scales for ac transport in semiconductor quantum dots include: the tunneling rate, $1/\tau \approx$ 10 MHz to 10 GHz; the transit time, $\hbar/\Delta E \approx$ 1 - 40 GHz, where ΔE is the single particle level spacing; the charging energy, $\hbar/(e/C) \approx$ 40 to 400 GHz, where C is the total capacitance of the quantum dot; and the plasmon energy, $\hbar\omega_p \geq 1$ THz. A significant challenge in experimentally probing these high-frequency regimes lies in the difficulty of coupling millimeter wavelength electromagnetic radiation to a sub-micron diameter semiconductor quantum dot.

In this chapter we introduce novel devices which integrate a local high-frequency oscillator directly with the nanostructure device which is under study. It consists of a superconducting Josephson junction incorporated on-chip with a quantum dot which is

formed electrostatically in a near surface two-dimensional electron gas (2DEG). The Josephson junction is a natural high-frequency voltage-tunable oscillator which is fabricated adjacent to the quantum dot. By means of an integrated coupling structure, the oscillating Josephson voltage signal can be capacitively coupled within an electronic phase coherence length of the 2DEG microstructure. The resulting high-frequency potential is strongly confined to the sub-micron active region of the quantum dot. We have developed a successful fabrication process and have demonstrated high quality Josephson junction oscillators integrated with semiconductor quantum dot devices.

5.2 Device Fabrication

A schematic of a completed integrated thin-film Josephson junction and quantum dot device is shown in Fig. 5.1, and a scanning electron micrograph of the finished device is shown in Fig. 5.2(a). The device consists of six metallic Cr:Au gates which are used to electrostatically define the quantum dot, one Josephson junction Nb/AlO_x/Nb trilayer, and the structure used to couple them at rf frequencies. The substrate is a GaAs/AlGaAs heterostructure containing a high-mobility two-dimensional electron gas 470Å beneath the surface. Fabrication of a completed device involves five successive patterning and processing steps aligned to within 100 nm of each other. The patterning is done by electron-beam lithography using PMMA resist and standard liftoff techniques. The following section provides a description of the processing techniques developed to fabricate the Josephson junction/quantum dot devices.

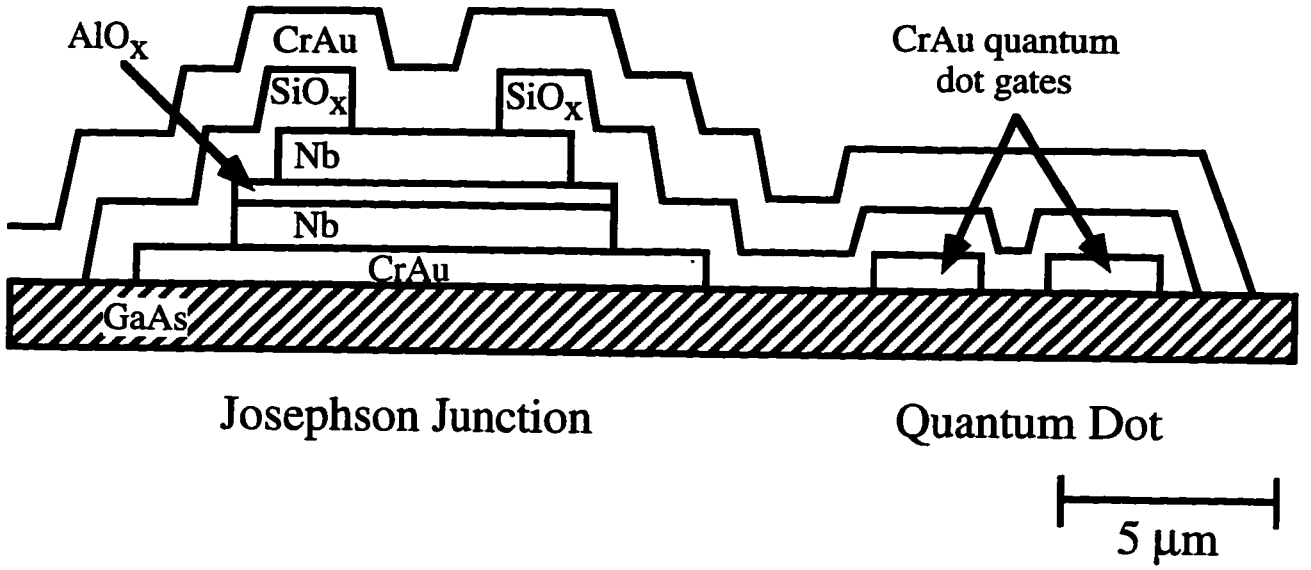


Fig. 5.1 Schematic of integrated thin-film device. The vertical scale is exaggerated for clarity.

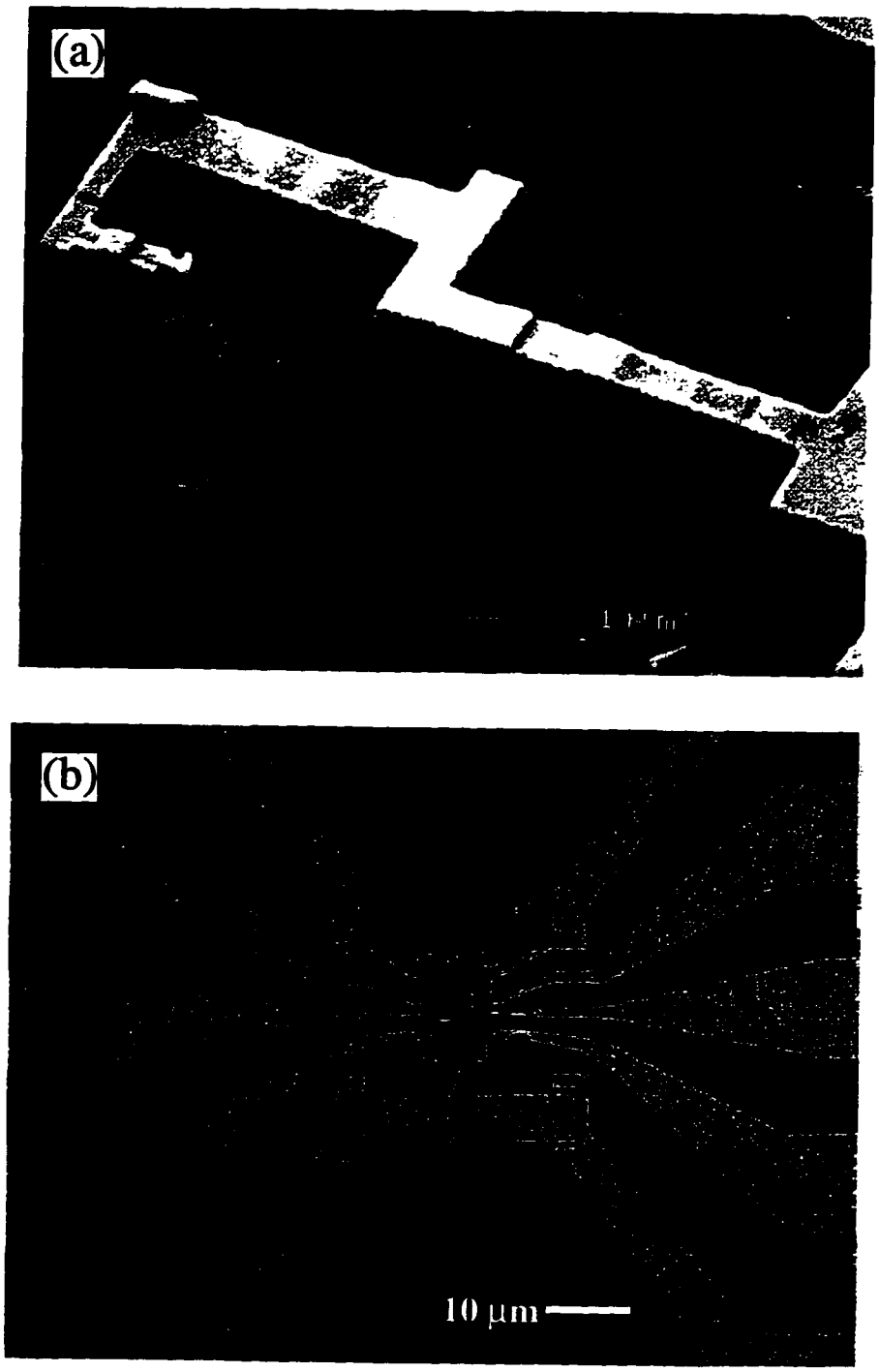


Fig. 5.2 (a) Scanning electron micrograph of completed Josephson junction/quantum dot device showing Josephson junction on the right and the gates used to define the quantum dot on the left, with the coupling structure connecting the two elements. (b) An expanded view optical micrograph of the same device. The Josephsopn junction is at the center of the image. Also visible are the alignment markers used at various magnifications during lithography.

1. Bottom Au:Cr Layer

The first step in device fabrication is patterning and deposition of the bottom Cr:Au metal layer. This layer has two primary purposes: (i) deposition of the surface electrostatic gates which will be used to define the quantum dot, and (ii) deposition of the bottom electrical contact pad onto which the Josephson junction trilayer will be placed; this contact pad also serves to prevent the Nb from being in contact with the GaAs surface and diffusing into the semiconductor. In addition, during this metallization step the alignment markers which will be used to align subsequent lithography steps are also patterned. The electron beam lithography and metallization for this step are identical to the process outlined in Chapter 2 for fabrication of surface gates for the parallel quantum dot devices. The thickness of this first layer is typically 300 Å (100 Å Cr, 200 Å Au), which is thick enough for the alignment markers to be visible through the layer of PMMA applied for the next lithography step.

2. Josephson Junction Trilayer Deposition

In order to maximize both the oscillation frequency and the output power of the Josephson oscillator, high current density tunnel junctions with large superconducting energy gaps are desirable. The Josephson junction in our device is a 10 x 10 μm^2 $Nb/AlO_x/Nb$ trilayer which was deposited in a dc plasma sputtering system in 10 mT of Ar without breaking vacuum. The primary consideration in selecting the size of the junction is that the dimensions be kept less than the Josephson penetration depth $\lambda_J \sim 15$ μm to avoid

self-field effects in the trilayer by which the tunneling current produces a magnetic field that affects the behavior of the junction. The Nb electrode thicknesses are both 1000 Å, which is larger than the 380 Å superconducting penetration depth of Nb. By sputtering the Al layer at a rate of 60 Å/min, pinhole-free AlO_x tunnel barriers of thickness 30 Å were deposited which resulted in high measured critical current densities of 1000 A/cm^2 [Gurvitch *et al.*, 1983; Morohashi and Hasuo, 1987]. An AlO_x barrier was chosen because of its excellent stability and low dielectric constant [Gurvitch *et al.*, 1983].

Since the total trilayer thickness is in excess of 2000 Å, a monolayer resist of 4% 496 K PMMA spun on at 3000 rpm and baked on the hotplate at 180 °C for 30 minutes was used. A bilayer of PMMA is unnecessary as the smallest feature written during this step is the 10 x 10 μm^2 trilayer. The 15 keV electron beam exposure parameters for the 10 x 10 μm^2 square junction written at 1000 magnification and 39 mm working distance are as follows: center-to-center spacing = 300 Å; beam current = 60 pA; area dose = 250 $\mu C/cm^2$. Liftoff of the trilayer, with the chip immersed in acetone, usually occurs in under one hour. The lithographic alignment required to place the trilayer in the desired location relative to the previously patterned Cr:Au layer was accomplished using the manual alignment technique detailed in the Nanometer Pattern Generation System Manual [Nabity, 1991; Yang, 1996].

3. SF_6 Reactive Ion Etch of Top Nb

The final 5 x 5 μm^2 junction is defined by a SF_6 reactive ion etch of the top Nb counter electrode using PMMA as an etch mask. Figure 5.3(a) is a scanning electron micrograph of the Nb/AlO_x/Nb trilayer after the SF_6 etch step. This etchback of the top Nb layer also serves to eliminate any electrical shorting which may have existed across the edges of the junction due to liftoff imperfections such as those seen in Fig. 5.3(a). The etch mask

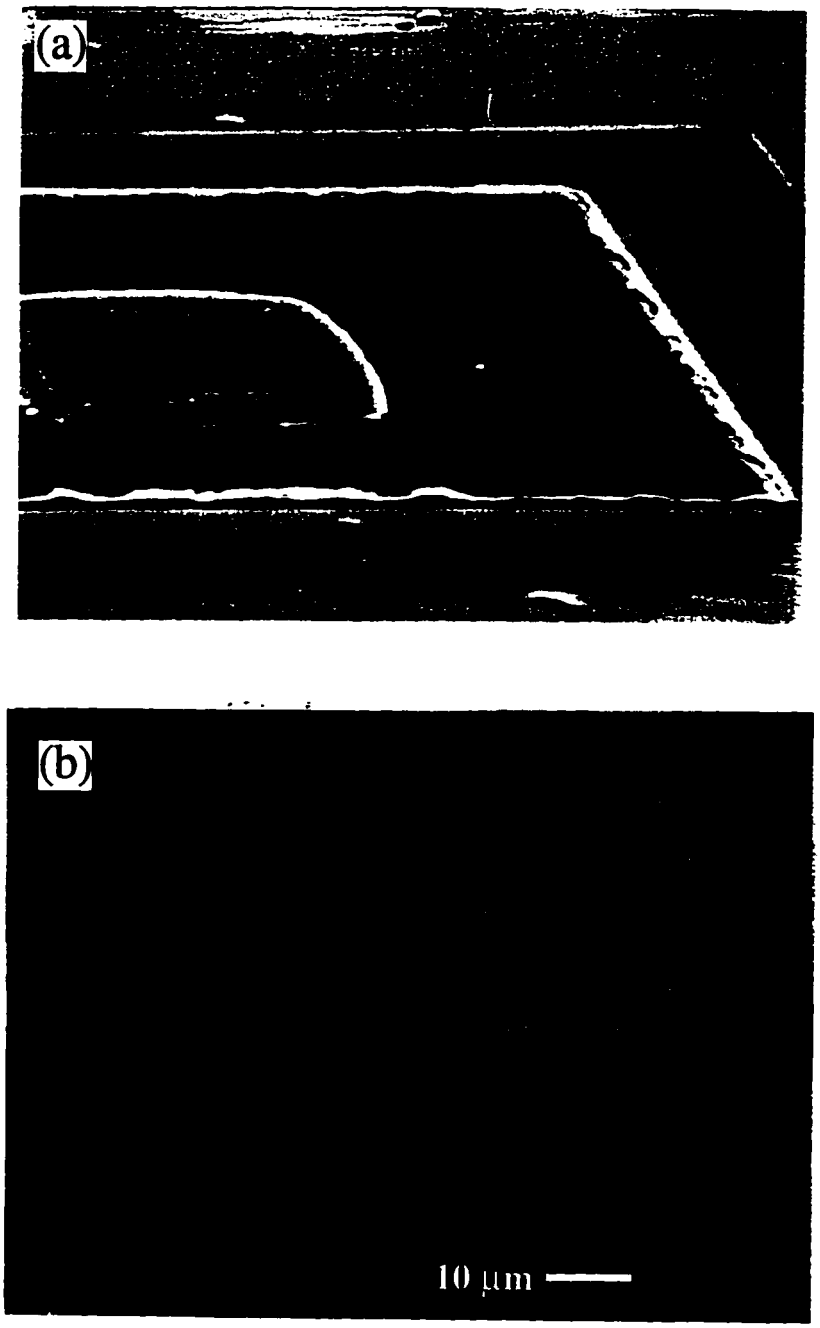


Fig. 5.3 (a) Scanning electron micrograph of the Nb/AlO_x/Nb trilayer after SF_6 reactive ion etch of the top Nb layer. Clearly seen are the ragged edges of the trilayer which would have caused electrical shorting of the junction. (b) Expanded view of the device after the SF_6 etch step.

consists of a trilayer of 6% 950 K PMMA, each layer spun at 3000 rpm and baked on a hotplate at 150 °C for 80 minutes. The hotplate bake temperature in this and all subsequent steps is lowered to 150 °C in order to prevent heat induced damage to the trilayer structure [Morohashi and Hasuo, 1987]. This yields a total PMMA thickness of approximately 20,000 Å. A very thick layer of PMMA is required to protect the masked wafer surface from the reactive ion etch because the SF_6 etches the PMMA at a rate of approximately 1700 Å/minute while etching Nb at a rate of 600 Å/minute. The details of the SF_6 reactive ion etch are given in Appendix B.

Figure 5.3(b) is an optical micrograph of the sample after the SF_6 etch step. The etched trilayer atop the previously deposited Cr:Au layer is visible at the center of the image, as are the Cr:Au alignment markers and the surface gates used to define the quantum dot. The bottom pair of arms in the micrograph will be used to make electrical contact to the top of the Josephson junction trilayer in the last metallization step.

4. SiO_x Insulating Layer Deposition

As seen in Fig. 5.1, after the etchback of the top trilayer Nb counter electrode an insulating layer of SiO_x is deposited over two edges of the Josephson junction. This is done to prevent shorting of the trilayer by the top Au layer which will form the electrical contact to the Nb counter electrode.

The SiO_x is deposited on the sample using the same general purpose thermal evaporator used for depositing the metallic surface gates. The SiO_x source consists of pellets of size of 2 mm to 4 mm (Cerac Coating Materials, Milwaukee WI) loaded into a baffled chimney boat (Model SM-8, J.D. Mathis Co., Long Beach CA). This boat design eliminates the danger of sputtered particles landing on the sample resulting in a non-uniform and leaky

dielectric film. For a reliable insulating film it was found that evaporation rates of 300 to 400 Å/minute are required. In addition, during evaporation the SiO_x boat becomes extremely hot, necessitating constant air-cooling of the evaporator sample stage during the deposition process. A SiO_x layer of approximately 4000 Å was deposited over the edges of the trilayer to ensure uniform coverage. SiO_x films of this thickness were separately tested for electrical insulation at 4 K and were found to have resistivities in excess of our measurement capabilities ($\rho > 10^6\ \Omega\cdot m$).

An identical thick trilayer of PMMA was used for this step as was used in the previous SF_6 step. Likewise, manual alignment was used to ensure that the SiO_x patterns covered the edges of the trilayer as required. Liftoff of the SiO_x film typically occurred in under one hour while immersed in acetone.

5. Top Cr:Au Layer

The final fabrication step involves thermal deposition of the top thick Cr:Au layer which makes electrical contact to the top of the Nb/AlO_x/Nb trilayer. The insulating SiO_x layer and the top Cr:Au layer also extend across the gates used to define the quantum dot in the 2DEG. Together with the bottom Au layer under the Nb base electrode this extension forms a transmission line which is capacitively coupled to the source and drain electrons in the 2DEG quantum dot. The top and bottom Cr:Au layers also aid in the removal of heat from the junction area to minimize self-suppression of the superconducting energy gap in the Nb electrodes under bias.

This last top Cr:Au layer, deposited in the thermal evaporator, is typically 7000 Å thick (200 Å Cr, 6800 Å Au) to ensure continuity across the vertical profile variations of the previously deposited films. The resist consists of a single layer of 4% 496 K PMMA spun

at 2000 rpm and baked on a hotplate for 45 minutes at 150 °C followed by two layers of 6% 950 K PMMA each spun at 3000 rpm and baked at 150 °C for 45 minutes. This resist profile has a thickness of approximately 15,000 Å while still providing an undercut to facilitate liftoff.

Figure 5.2(a) and (b) are micrographs of a completed device. The coupling structure is seen in the closeup view of Fig. 5.4(b). Figure 5.4(a) shows a closeup view of the Josephson junction trilayer after the final top thick Cr:Au electrode is deposited. These features will be discussed in detail in the following sections.

5.3 Josephson Junction Characteristics

A typical current-voltage (I_{bias}-V_{dc}) curve of an on-chip 5 x 5 μm^2 Josephson junction at 4.2 K is shown in Fig. 5.5. The observed gap sum value (2.3 mV), a measure of the quality of the Nb films, is somewhat reduced compared to the clean Nb value of $2\Delta(0) = 3.1$ mV [Orlando and Delin, 1991] due to proximity effect with metallic Al in the barrier and impurities in the Nb film. The normal state resistance and the critical current of the junction are measured to be $R_n = 1.2\ \Omega$, and $I_c = 0.9$ mA respectively. As is expected for a planar geometry, the junction capacitance leads to a hysteretic current-voltage curve symmetric about the origin. When a dc voltage bias is applied across the Josephson junction it will produce an oscillating voltage signal at a frequency determined by the Josephson relation

$$f = 2eV_{dc}/h \qquad (5.1)$$

where V_{dc} is the average dc voltage across the junction. Experimentally, we current bias the Josephson junction so that $V_{dc} = I_{bias} R_n$, where I_{bias} is the applied current bias. An

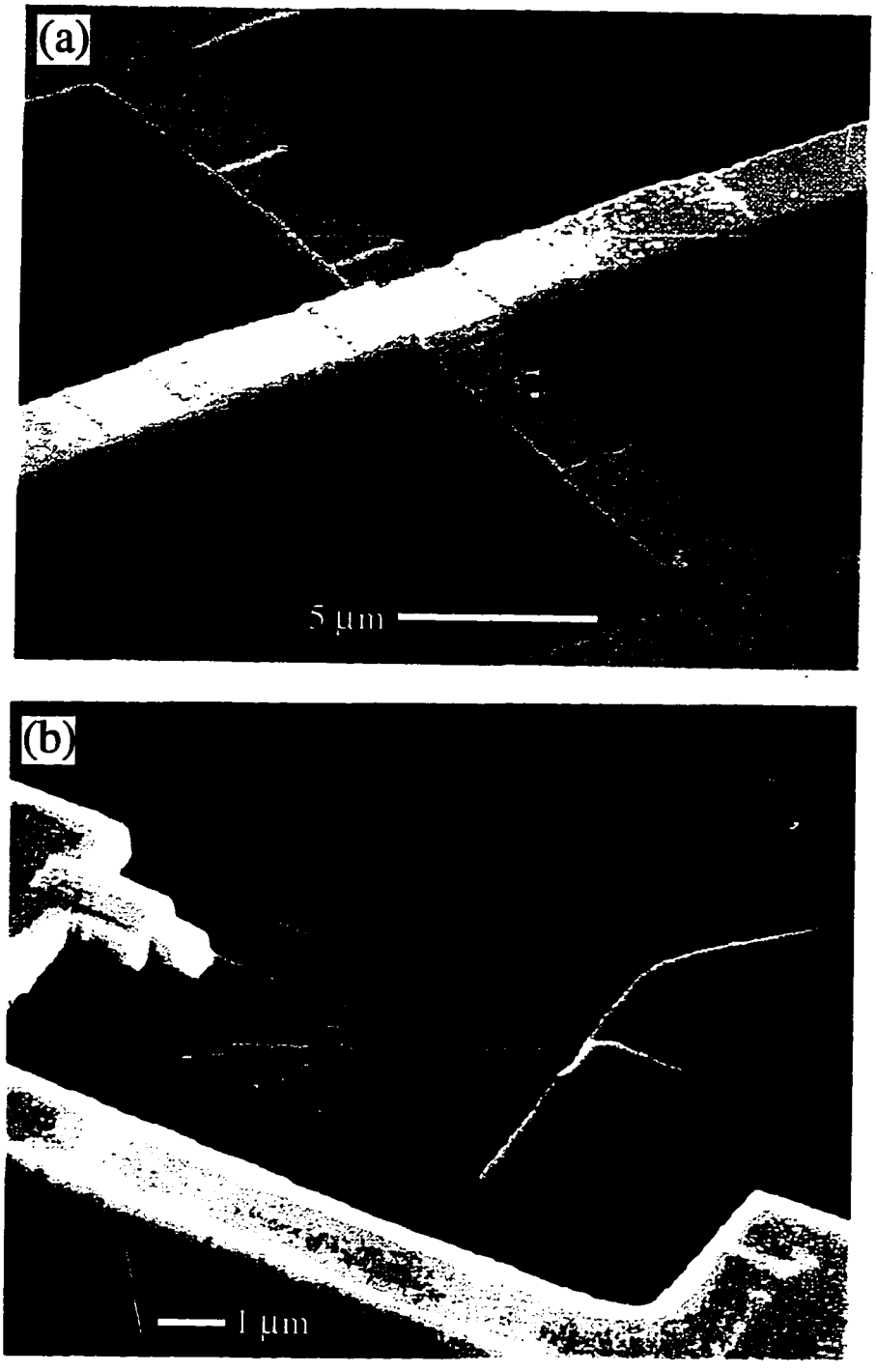


Fig. 5.4 (a) Scanning electron micrograph of a completed Josephson junction. The outer square perimeter is the 10 μm x 10 μm deposited trilayer, and the inscribed smaller square is the 5 μm x 5 μm top Nb counter electrode after the SF_6 etch step. The bright white feature is the thick Cr:Au electrode deposited in the last step. (b) An expanded view of the quantum dot region of the device showing the ends of the coupling structure. See Fig. 5.6 for the equivalent circuit diagram.

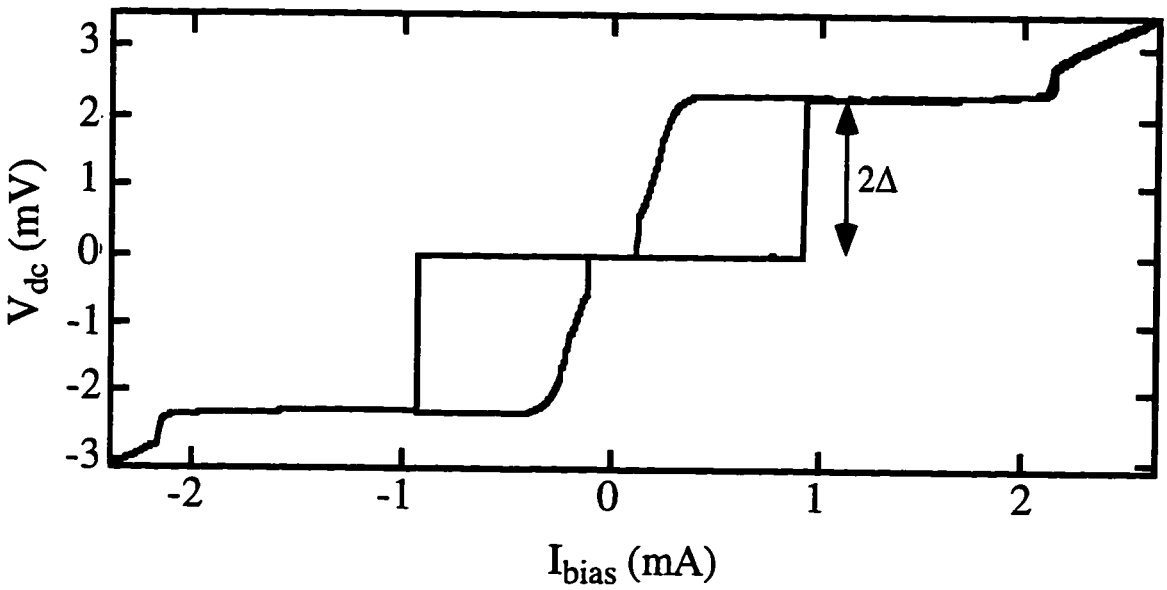


Fig. 5.5 Current-voltage characteristic of a completed 5 μm x 5 μm Josephson junction at 4.2 K, $I_c = 0.9$ mA, $R_n = 1.2$ Ω. The features of the data are discussed in the text. The gap sum value as indicated in the figure is $2\Delta \approx 2.3$ mV.

upper limit on the operating frequency of our Josephson oscillator is set by the superconducting gap of the Nb, which in this case corresponds to 1.1 THz; a typical operating frequency is 300 GHz, corresponding to $V_{dc} \approx 1$ mV in Fig. 5.5. At this frequency the signal wavelength is $\lambda_{eff} \approx \lambda_o((\varepsilon_{GaAs} + 1)/2) = 380$ μm, taking into account the dielectric constant of the GaAs half-plane $\varepsilon_{GaAs} = 13.1$, which is much longer than the 10 μm length of transmission line between the Josephson oscillator and the quantum dot. As a result, the phase of the signal across the length of the coupling structure is approximately constant and we may use a simple ac circuit to model the device.

5.4 Equivalent Circuit Model

The equivalent circuit of the integrated Josephson oscillator and quantum dot is shown in Fig 5.6. L_p and C_p are the parasitic inductance and capacitance of the combination of the planar Josephson junction and the coupling structure, and C_c represents the capacitance between the open end of the coupling structure and the electrons in the 2DEG beneath the surface. A detailed view in the vicinity of the quantum dot is shown in Fig. 5.4(b). The ends of the coupling structure need to be within an electronic phase coherence length ($\ell_\phi \sim$ 1 μm for $T_e \sim 1$ K) of the quantum dot in order for the high frequency field to influence electron transport through the device. For the dimensions shown in Fig. 5.3(a), we estimate a parasitic inductance of $L_p = 1.3$ pH. The magnitude of the oscillator signal across the 2DEG, V_{ac}, will be determined by the total capacitive loading of the Josephson oscillator. When the McCumber parameter β_c, defined by [Orlando and Delin, 1991]

$$\beta_c = (2e/\hbar)(I_c R_n)(R_n C_p) \qquad (5.2)$$

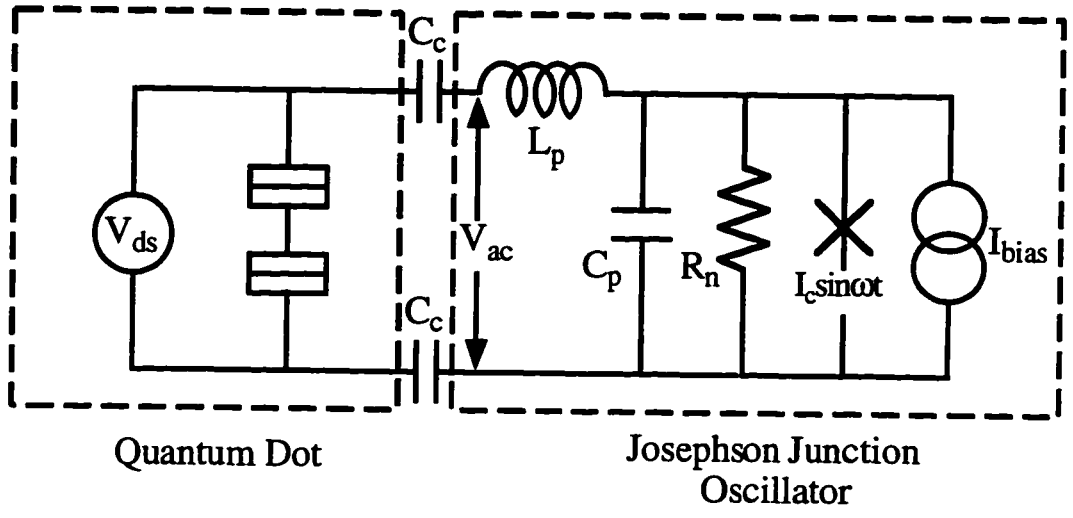


Fig. 5.6 Equivalent circuit model of Josephson junction/quantum dot device as discussed in text. The current biased Josephson junction is represented by a Josephson supercurrent element $I_c \sin\omega t$ in parallel with the junction normal resistance R_n. C_p and L_p are the parasitic capacitance and inductance, respectively, of the trilayer and coupling structure.

is less than unity the junction is not capacitively shunted and the maximum ac voltage obtainable is $V_{ac} \approx I_c R_n$ = 1.1 mV, at least for $V_{dc} < 2\Delta/e$. The capacitance C_p in expression (2) is dominated by the capacitance of the planar junction. For a 5 x 5 μm^2 trilayer junction with an AlO_x barrier 30Å thick this capacitance is C_p= 2.1 pF, using $\varepsilon_{Al_2O_3} = 8$ for the dielectric constant of the AlO_x barrier. This gives $\beta_c = 7$, so the ac voltage signal is partially shunted, with the 3 dB point at 80 GHz, and the *I-V* curve is hysteretic. Using this value of β_c, at a typical operating frequency of 300 GHz the magnitude of the oscillating potential expected across the quantum dot is approximately $V_{ac} \approx 50\ \mu V$.

5.5 Results and Comments

Josephson Junction/Semiconductor Microstructure Devices

Using the processing techniques described above, six complete devices were fabricated: samples 1 through 3 are Josephson junctions coupled to quantum dots, and samples 4 through 6 are with Josephson junctions coupled to single quantum point contacts. Each of the Josephson junctions on the six devices exhibited high-quality behavior similar to Fig. 5.5. The range of critical currents I_c observed across the six samples, all of which had Josephson junctions of final size 5 μm x 5 μm or 10 μm x 10 μm after the SF_6 etch step is shown in Table 5.1, representing a high degree of uniformity resulting from the fabrication process. A similarly uniform range of normal resistances R_n was observed for the barrier thicknesses, as summarized in Table 5.1.

Sample	Junction Size	Barrier Thickness	I_c (mA)	J_c (A/cm^2)	R_n
1	$10 \times 10\ \mu m^2$	60 Å	0.7	700	0.7 Ω
2	$5 \times 5\ \mu m^2$	40 Å	0.8	3200	1.1 Ω
3	$5 \times 5\ \mu m^2$	30 Å	1.0	4000	1.0 Ω
4	$5 \times 5\ \mu m^2$	30 Å	1.2	4800	0.9 Ω
5	$5 \times 5\ \mu m^2$	30 Å	0.9	3600	1.2 Ω
6	$5 \times 5\ \mu m^2$	30 Å	0.9	3600	1.1 Ω

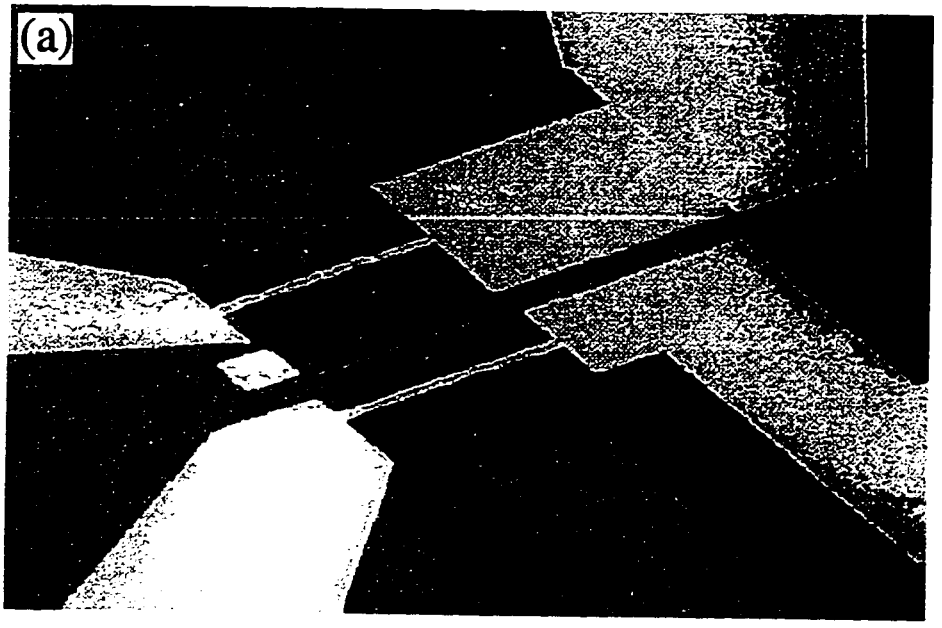
Table 5.1 Summary of Josephson junction characteristics for the six completed Josephson junction/semiconductor nanostructure devices. The Josephson junction size refers to the final size of the junction after the SF_6 etch step.

Each of the samples was measured in either a ^{3}He refrigerator with a base temperature of 300 mK, or a ^{3}He/^{4}He dilution refrigerator with a base temperature of 35 mK (see Chapter 2 for dilution refrigerator details). Low temperatures are required to see discrete photon effects since a frequency of f = 100 GHz, a typical operating frequency of the Josephson junction oscillator, corresponds to a temperature of $T = hf/k_B = 5$ K. Of the three samples with quantum dots, one sample exhibited stable Coulomb blockade charging behavior, albeit in a limited range of gate voltage (for a detailed explanation of Coulomb blockade charging effects in quantum dots see Chapters 3 and 4). All of the three quantum point contact samples exhibited working point contacts whose channels pinched off with sufficiently negative gate voltage bias, but only one of the devices exhibited clean conductance plateaus.

Measurement Results

The photoresponse of each of these samples was measured by activating the Josephson junction and monitoring the dc transport current through the quantum dot or the quantum point contact. Measurements were performed using two methods: (i) by continuously activating the Josephson junction and comparing the recorded conductance data to data taken without the Josephson junction activated, and (ii) by chopping the bias current to the Josephson junction at a frequency of 27 Hz and measuring the response at that frequency, which allows a simultaneous measurement of the total current and any photocurrent. Despite the use of both these methods, no influence of the Joesphson junction oscillator, operated over a range of frequencies from 100 GHz to 500 GHz, was observed in any of the samples. Any photocurrent which would have been present may also have been masked by the inherent switching noise instability present in these semiconductor samples (see Sec. 4.3).

We attribute the failure to see any effects due to the Josephson oscillator to the low output ac voltage amplitude V_{ac}, which was estimated in Sec. 5.4 to be approximately $V_{ac} \approx 50\ \mu V$ at $f = 300$ GHz. To test this hypothesis, we fabricated a sample consisting of two adjacent capacitively coupled Josephson junctions, shown in Fig. 5.7(a). The thin film coupling capacitor, consisting of two Cr:Au layers separated by a SiO_x dielectric layer, is the structure at the top right of the micrograph, and has a calculated value of $C_c = 1$ pF. As before, since the wavelength of the ac signal is much larger than the device size ($\lambda \approx 400\ \mu m$), we are justified in using a discrete element circuit model. The equivalent circuit for this device is shown in Fig. 5.7(b). The device is designed to use one of the Josephson junctions as a high-frequency oscillator, while the neighboring capacitively coupled Josephson junction acts as a detector. The *I-V* characteristics of the detector should



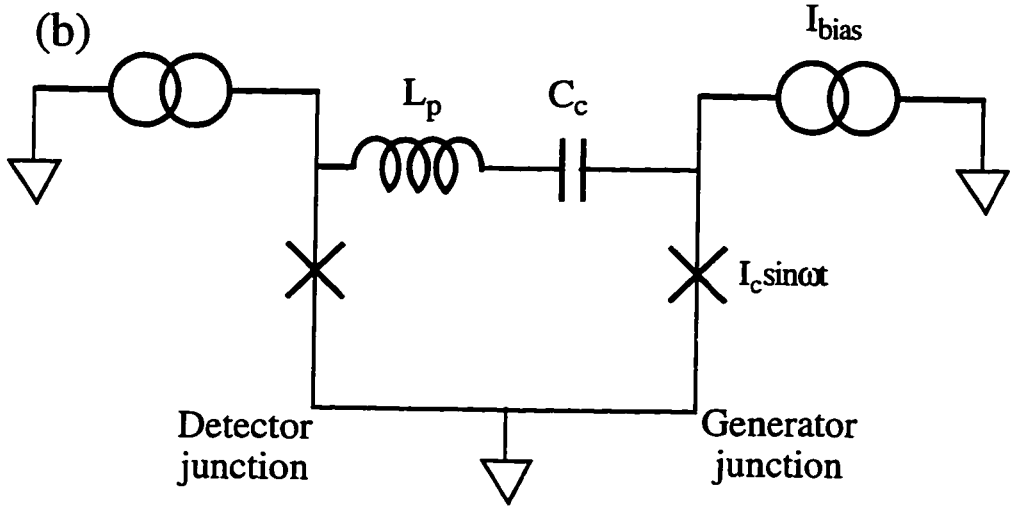


Fig. 5.7 (a) Scanning electron micrograph of device consisting of two adjacent Josephson junctions capacitively coupled at rf frequencies. The coupling capacitor is visible at the top of the image. The dark areas are the SiO_x insulating layer. (b) Equivalent circuit model for coupled Josephson junction device. Josephson junctions are denoted by crosses. C_c is the coupling capacitance and L_p is the parasitic capacitance of the coupling structure. Both junctions are current biased.

exhibit current steps, known as Shapiro steps, at voltages $V = n\hbar\omega_g/2e$, where n is an integer and ω_g is the frequency of the generator junction, due to photon-assisted tunneling induced by the high frequency produced across the detector junction [Van Duzer and Turner, 1981]. The current steps are predicted to have amplitudes $I_c J_n(2eV_{ac}/\hbar\omega_g)$, where the J_n's are Bessel functions of the first kind, I_c is the critical current of the detector junction, and V_{ac} is the amplitude of the high frequency ac voltage across the detector junction.

The coupled Josephson junction device was measured in a ^{3}He refrigerator at 400 mK. With the generator junction biased over its entire range, no Shapiro current steps were exhibited by the detector junction. This null result does however provide an upper bound on the amplitude of the ac voltage V_{ac} which is produced by the generator junction, since the minimum detectable current level in the measurement was 10 μA, limited largely by the inherent instability due to thermal fluctuations in the Josephson junction which resulted in switching between zero voltage and finite voltage states. With this measurement limit, we calculate $V_{ac} < 10$ μV, within a factor of 5 of the predicted maximum value of $V_{ac} \approx 50$ μV.

Future Improvements

The need to increase the output ac voltage of the Josephson oscillator in the Josephson junction/quantum dot devices is clearly a priority for successful operation of these devices. One possible method to increase the ac output voltage of the Josephson oscillators is shown schematically in Fig. 5.8(a). As shown in the corresponding circuit model of Fig. 5.8(b), by appending an open circuit transmission line to the Josephson junction which at certain frequencies acts as an inductance in parallel with the junction, the inherent capacitance of

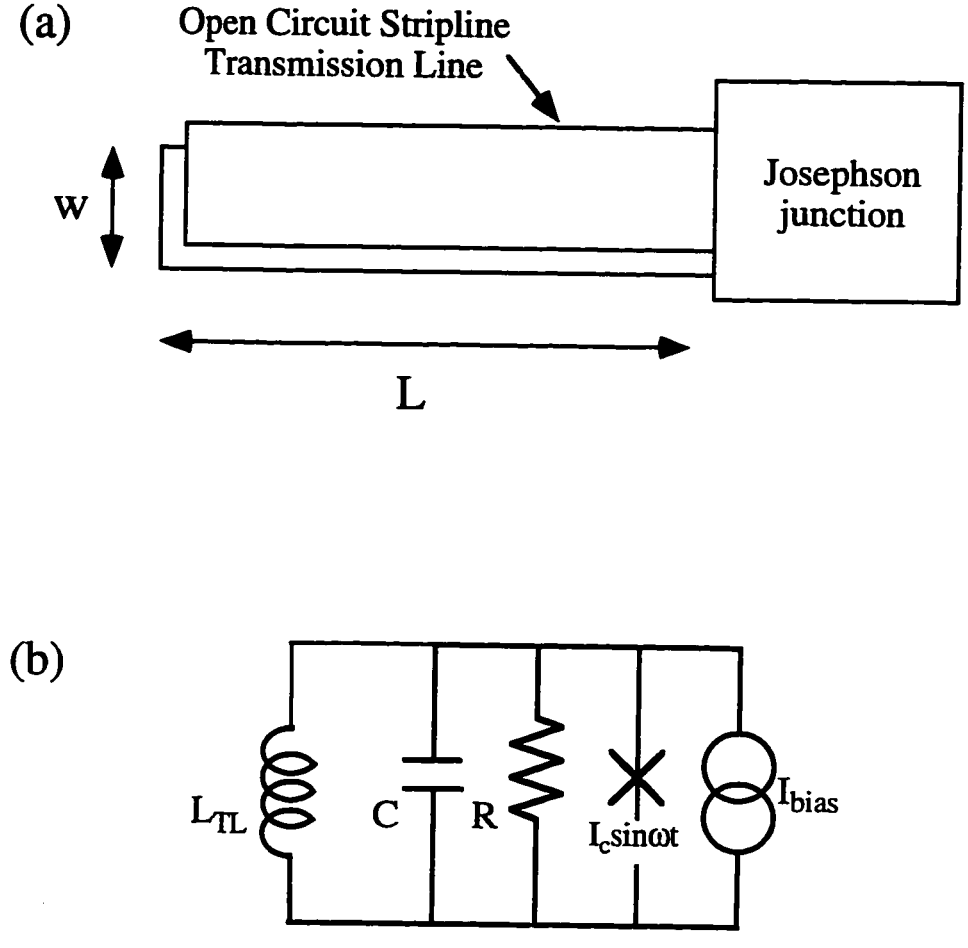


Fig. 5.8 (a) Schematic illustration of an open circuit stripline transmission line with characteristic impedance Z_o appended to a Josephson junction trilayer. (b) Equivalent circuit of Josephson junction with inductance L_{TL} of transmission line. At the resonant frequency, the inductance L_{TL} will tune out the junction capacitance C, leaving the junction resistance R as the effective junction impedance.

the junction trilayer, which is the primary origin of the capacitance which is shunting the available ac voltage output, will be tuned out, leaving only the junction resistance R_n in parallel with the Josephson supercurrent element and resulting in the maximum ac voltage amplitude attainable $V_{ac} = I_c R_n \approx 1$ mV. The impedance of an open circuit transmission line of length L and characteristic impedance Z_o for a wavelength λ is given by [King, 1955]

$$Z_{oc}(L) = -jZ_o \cot(2\pi L/\lambda). \qquad (5.3)$$

The resonance condition is that the sum of the impedances of the junction capacitance and the transmission line equal zero:

$$\omega C + (1/Z_o) \tan(2\pi L/\lambda) = 0. \qquad (5.4)$$

If the dielectric material in the transmission line is AlO_x, which would be the most compatible with the Josephson junction fabrication process, at a typical operating frequency of 300 GHz, $\lambda = \lambda_o/\sqrt{\varepsilon_{AlO_x}} \approx 450$ μm. Choosing $(2\pi L/\lambda) = 0.75\pi$ leads to a transmission line length of L = 170 μm. Furthermore, a typical characteristic impedance value of $Z_o = 4$ Ω implies a thickness of the AlO_x dielectric in the transmission line of $t_{AlO_x} = 3000$ Å and a width w = 35 μm, which are dimensions readily compatible with the existing fabrication and processing methods. The drawback to this solution is, however, that it limits the operation of the device to only those frequencies for which Eqn. (5.2) is satisfied.

5.6 Summary

In summary, we have presented a new mesoscopic device which incorporates on-chip a local Josephson junction oscillator. We have developed a process for fabricating these multi-layer integrated devices which results in high-quality Josephson junctions with characteristics well-suited to their use as high-frequency sources. By coupling an on-chip local oscillator to a single mesoscopic device we eliminate the need for external sources of radiation and the issues involved with transmitting a signal into a cryostat. The on-chip Josephson oscillator should be able to provide a strongly localized time-dependent voltage over a frequency range from a few hundred gigahertz to over 1 THz, allowing the study of a variety of time-dependent phenomena in electron transport through mesoscopic structures.

Concluding Remarks and Future Directions

This thesis has described experimental low temperature measurements performed on a coupled quantum dot system in the Coulomb blockade regime. The device studied consists of two dots in a parallel configuration situated sufficiently close together to allow significant interaction with each other. In particular, the experiments were designed to probe explicitly the role of quantum mechanical interdot coupling in the double dot system. The device geometry allowed for a systematic study of these effects at various distinct regimes of interdot interaction.

The experimentally measured charging characteristics of the parallel coupled dot device presented in Chapter IV were seen to agree well with the theoretical model introduced in Chapter III which included the role of quantum mechanical interdot charge fluctuations in calculating the conductance through the device. With the two dots very weakly coupled, it was seen that changes in the electrostatic potential of one dot became observable in the conductance as measured through the neighboring dot. Exchange of particles by quantum mechanical tunneling between the dots was seen to lead to a reduction of the internal charge polarization of the system, leading in turn to the appearance of secondary peaks in the Coulomb blockade spectrum as measured through only one dot. Measurements of the temperature dependence of these secondary peaks provided evidence that the origin of the quantum charge fluctuations is likely inelastic cotunneling for low interdot conductances. Further experiments performed in which the conductance through both dots was measured simultaneously provided direct evidence that these secondary peaks correspond to changes in the charge state of the adjacent quantum dot. In particular, the experimental results

verified the striking prediction that the coupled dot system behaves as a single composite dot with exactly $2e^2/h$ of conductance between the dots.

There exist many promising areas for future work in the study of multiple interacting quantum dots. For systems consisting of two coupled dots, we have seen that one of the dots can act as a highly sensitive detector, sensing changes in the electrostatic potential of the other dot. It would be particularly interesting to investigate whether such a detector can function in the time domain. In such a device it might be possible to detect changes in potential arising from fluctuations in the number of electrons as current flows through a quantum dot. Systems of three or more quantum dots arranged in novel geometries will allow the study of electronic phase coherence phenomena both in the absence and in the presence of an applied magnetic field.

From a more technological perspective, it has recently been suggested that it may be possible to realize a cellular automata device in a configuration of coupled quantum dots. In such a device the switching results from the change in the quantum mechanical ground state configuration arising from external polarization charges. Recent efforts have also been directed toward the development of single-electron ultra high-density memory [Yano, 1993]. It is difficult however to envision the development of truly practical applications for any quantum effect device until the operating temperatures can be raised. The temperature at which Coulomb charging effects become observable could be raised by reducing the effective capacitance which determines the charging energy. Such a reduction in capacitance might be achieved by a further reduction of device dimensions, using etching rather than gating to achieve confinement, or exploring different material systems such as silicon or Al/AlO_x metallic structures. All of these are current areas of active research.

APPENDIX A

Kelvinox 100 Dilution Refrigerator Operation

This appendix details the procedures developed for successfully cooling down and operating the Oxford Kelvinox 100 dilution refrigerator system on the second floor of Gordon McKay Laboratory. These procedures have been optimized for the particular system we have, and may differ in some respects from those suggested in the Kelvinox Operator's Handbook supplied by Oxford Instruments.

Final Assembly

Before mounting the sample on the mixing chamber tailpiece (described in chapter 2) it is wise to perform a room temperature check of the electrical measurement wiring for continuity (from the BNC box attached to the Fischer connectors at the top of the insert to the sample leads down at the tailpiece), shorts to ground, and inter-lead shorts. Any loose wires or slack should be tied flush to a nearby solid post inside the insert using dental floss (do not use tape, as this will strip the wire insulation) in order to reduce vibrationally induced noise and to avoid a thermal short between the wiring and the inner wall of the radiation shield or the inner vacuum can (IVC). Similarly, it is important to check that the tailpiece is well aligned with the mixing chamber cold finger, avoiding any potential contact between the tailpiece and the radiation shield or the IVC. The experiments described in this thesis were performed both with and without the radiation shield, with no observable

difference in sample performance. It is also a good idea to check the insert thermometry by attaching the cable from the AVS-46 resistance bridge to Fischer connecter #1 and verifying that all seven thermometers are reading their correct room temperature values (expect ~10% deviation from the recorded values).

The IVC is mated to the insert using a greased cone seal. To maintain the integrity of the seal, it is critical not to introduce any scratches on either of the seal surfaces. The old grease from the previous cool down should always be removed from both the IVC inner surface and the flange surface on the insert before applying fresh grease to the seal. This can be done using an index finger while wearing powder-free PVC gloves to wipe the surfaces clean, always wiping parallel to the seal top; never use tissues or any other wipes which may introduce particles on the seal surfaces. Once the surfaces are clean, apply fresh Dow-Corning High Vacuum Grease thoroughly to both the surface on the insert (roughly 1" squeezed from a 150g tube) and to the seal surface on the inside of the IVC (about 1/2" from 150g tube), using new powder-free PVC gloves.

In anticipation of leak checking the IVC cone seal, the leak detector is attached to the IVC pumping port at the top of the insert. The IVC is then carefully fitted over the insert, being careful not to scrape the inside surface of the IVC against any part of the insert. The seal is set by pushing the IVC onto the cone seal with a slight twisting motion and then pumping on the IVC space with the leak detector. The extruded grease can be removed or spread around the seal. It is not possible to separate the IVC once the cone seal has been formed without using the slide hammer; the locking taper prevents separation of the IVC even if the insert is vented to atmospheric pressure. The cone seal can then be leak checked by spraying He around the seal. Before lowering the insert into the dewar, the 1K pot fill tube should be securely taped to the IVC using yellow mylar tape (CHR Industries Inc., New Haven, CT) to prevent damage to the insert or the dewar during insertion.

After the cone seal has been proven to be leak tight, He exchange gas is introduced into

the IVC (if a throughput test and dilution unit leak test are to be performed however, this step is delayed until after those tests are completed). The amount of He exchange gas is not critical; typically one meter of flexible rubber hose filled with He is used (the hose should be evacuated first, then slightly overpressurized, to minimize the amount of air getting into the IVC). The IVC valve at the insert is then closed, all pumping lines disconnected, and the insert is raised to the ceiling through the hatch at the top of the screen room using the hand crank, being extremely careful not to crash any part of the insert into either the screen room ceiling or the room ceiling. After positioning the dewar underneath the hanging insert (there is a circle marked on the floor indicating the proper placement) the insert is slowly lowered, making sure that it does not get caught on its way down either on the baffles inside the dewar or on the wooden shelf on the wall. Once the insert is fully lowered, it can be properly aligned (by rotating, noting the alignment markers on the dewar neck) and secured to the dewar using the fastening bolts.

The still line, condenser line, and 1K pot pumping line are attached to the insert using non-conducting plastic O-rings and clamps. The pipe from the cabinet intended for the IVC should be blanked off and clamped, as it will not be used in any subsequent steps. To evacuate and leak test the still and condenser lines, the leak detector is attached to the cabinet via the pipe which is branched off from the port in the cabinet rear labeled 'IVC/OVC' (there is also a valve at the end of this pipe behind the cabinet). The still and condenser lines are evacuated by opening valves 2A, 7, 2, 3 and 1 to the leak detector pump (with 5A closed); it is important that the still and condenser valves at the top of the insert remain closed to protect the dilution unit from atmosphere. After pumping for a few hours (P1 should reach less than about 5×10^{-2} mbar) and leak testing the still and condenser lines and joints, it is a good idea to pump on the dilution unit (before opening still and condenser valves at the top of the insert, protect the leak detector by temporarily closing valve 7). There should be very little pressure in the dilution unit, as it should not

have been vented to atmosphere at any point. The dilution unit should be evacuated to a pressure less than 5 x 10^{-2} mbar on gauge P1, and then closed off with the insert still and condenser valves. Before cooling the insert to 77 K, an optional throughput test and dilution unit leak check can be simultaneously performed; see the checklist for the procedure.

Cooling to 77 K

Immediately before cooling to 77 K it is important to pump out the 1 K pot, through valve 4A, since there is a small known leak through the 1 K pot fill tube. The needle valve and valve 1A should be closed. The main bath is filled with liquid nitrogen using the stainless steel blow-out tube inserted into the transfer port at the top of the dewar (the tapered end of this tube mates with a siphon cone inside the bath to direct the liquid flow to the bottom of the dewar). The value of the resistor fixed to the top of the magnet will indicate whether the liquid nitrogen level has risen above the magnet (the resistor is connected to pins E-J on connecter B of the dewar; the resistor values are 139 Ω at 300 K and 174 Ω at 77 K, as of this writing). Once the nitrogen level reaches the top of the magnet, the dewar is filled for a few more minutes and then left to pre-cool thoroughly. The cooling can be monitored using the diagnostic thermometry on the insert. Several hours are required to cool the insert to 77 K; it is typically convenient to let it cool overnight.

Once the diagnostic thermometers show a temperature close to 77 K, an optional throughput test and dilution unit leak check can be performed, following the same procedure as at room temperature. The liquid nitrogen is removed from the dewar by inserting the blow-out tube into the transfer port and slightly overpressurizing the bath with He gas. This can be conveniently done by attaching the pipe from the 'Main Bath' port at

the rear of the cabinet to the dewar exhaust port, with the He gas supplied through a valved hose nipple placed between the pipe and the cabinet. A constant downward push needs to be applied to the blow-out tube to force the tapered end into the funnel inside the dewar and ensure a good seal. The outflowing nitrogen can be directed into the nitrogen trap dewar. Once the flow of nitrogen stops, the bath is pumped out by attaching the pipe from the 'Main Bath' port at the rear of the cabinet to the dewar exhaust port and using the rotary pump through valves 4A and 1A, making sure 5A, 2A, 3A and the 1 K pot valve at the insert are all closed. The bath pressure is indicated by G3. Pumping slowly by throttling 4A prevents overloading of the rotary pump. If there is any liquid nitrogen left at the bottom of the dewar, the pressure read by G3 will hesitate around 100 mbar, in which case the dewar should be repressurized with He and reevacuated. After all the liquid nitrogen is blown out, the bath is repressurized with He gas and the dewar exhaust pressure relief valve reattached.

Cooling to 4.2 K

The 1 K pot is again evacuated before cooling down to 4.2 K (making sure that the pumping line is evacuated before opening the valve at the insert). The initial liquid helium transfer should be very slow; if the exhaust frosts excessively expensive enthalpy is being wasted. It takes approximately 20 liters of liquid He to cool the cryostat to 4 K, and 40 liters to fill the dewar. After the initial transfer is completed and the diagnostic resistors approach the 4 K values, the He exchange gas in the IVC can be pumped out using the turbopump on the leak detector attached directly to the IVC pumping port at the top of the insert (using a single length of piping improves pumping efficiency). The exchange gas is conveniently pumped out overnight, until the helium leak signal on the leak detector is less

than 3 x 10^{-7} atm cc/s. The procedure for condensing the mixture and starting circulation are detailed in the checklist section below.

Abridged Operating Procedures

Cooling to 77 K

- Remove old grease from cone seal and apply new grease.
- Fit IVC over insert and form cone seal.
- Test IVC cone seal for leaks at room temperature.
- Secure 1K pot fill tube to IVC with mylar tape.
- Perform throughput test / dilution unit leak check as described below. *(optional)*
- Introduce He exchange gas into IVC.
- Lower insert into dewar, align, and secure using fastening bolts.
- Attach still, condenser, and 1K pot pumping lines to insert; make sure pipe from cabinet intended for IVC is blanked off.
- Attach leak detector to cabinet "IVC/OVC" port branch and evacuate still, condenser and 1K pot pumping lines through 2A, 7, 2, 3, 1 to P1 < 5 x 10^{-2} mbar.
- Leak check lines and joints.
- Open still and condenser valves at top of insert and pump dilution unit to P1 < 5 x 10^{-2} mbar.
- Close still and condenser valves at top of insert and all valves on cabinet; detach leak detector from cabinet.
- Perform optional room temperature throughput test and dilution unit leak test (see

procedure below).

- Evacuate 1K pot through 4A; make sure needle valve and 1A are closed.
- Transfer liquid nitrogen into dewar. Watch value of resistor E-J on connector B change to be sure that level is above top of magnet.
- Wait until thermometry reads 77 K; typically let cool overnight.
- Perform optional 77 K throughput test and dilution unit leak test (see procedure below).
- Attach 'Main Bath' pipe with valved hose attachment to dewar exhaust.
- Overpressure dewar with He gas through 'Main Bath' pipe and blow out liquid nitrogen.
- Withdraw blow out tube, insert bung, and pump out bath using rotary pump through 4A and 1A, making sure 5A, 2A, 3A and 1K pot valve at insert are all closed.
- If G3 hesitates around 100 mbar, there is still some liquid in bath. Repressurize bath and repeat pump down.
- Repressurize bath to atmosphere with He gas.

Cooling to 4.2 K

- Evacuate 1K pot through 4A; make sure needle valve and 1A are closed. Stop pumping once 1 K pot is empty.
- Open dewar exhaust and transfer liquid helium slowly (typically longer than 1-2 hours). It takes ~ 60 liters to cool and fill bath.
- When thermometry reads 4 K, pump He exchange gas from IVC by attaching leak detector directly to IVC port at insert. Pump overnight until leak signal is less than $3x10^{-7}$ atm cc/s.

Condensing and Circulating Mixture

- Turn on He rotary pump and check the oil level (this pump requires special oil- contact Oxford for details).
- Clean traps by pumping on them through 5A, 2A, 7 and 11A (with all other valves on panel closed) while warming nitrogen trap thoroughly with heat gun. It is essential that the pump is not removed during heating, as high pressures can develop in the traps. Close all valves once traps are clean and back at room temperature.
- Cool nitrogen trap by inserting it in its dewar. Cool helium trap by inserting it in a full 60 liter storage dewar.
- Fill and pump on 1 K pot by opening needle valve ~1/4 turn and opening 4A and 1K pot valve at insert. R6 should settle to 650-700 Ω, and P2 should read 6-10 mbar, after a few minutes.
- At insert, open only still valve; mixture will be condensed on still side.
- Open 3.
- Open 13a and let mixture from behind pumps cool in traps for ~1 minute.
- Open 12a and let precooled mixture into still line.
- Open 9 and dumps valve to allow dumps mixture into circuit. Check that still is cooling by noting increase in R2.
- After ~1 hour close 9 and open 10 slowly, keeping G2 < 400 mbar, to pump remaining mixture out of dumps.
- It will take 1-2 additional hours to condense mixture (impedance of He trap is high); the longer you wait, the easier it will be to start circulation.
- To start circulation: open 1 and condenser valve at top of insert, close 3 and 10, and open 6 by cracking the valve very slowly, keeping G2 < 400 mbar (at this point, 2, 3,

4, 5, 7, 8, 9, 10, 11a should all be closed). Keep cracking 6 until it is all the way open. Be patient; this may take more than half an hour.

- Operate resistance bridge at 30 μV excitation, and watch R4 and R7 values rise. It will take a few hours to reach base temperature.
- The still heater can be adjusted to 0.5 - 1.0 mW to decrease base temperature.

Daily Maintenance

- Transfer liquid He daily, keeping level above 30% to ensure 1K pot remains filled.
- Replenish liquid nitrogen trap twice daily.
- Perform a 'quick clean' of the helium trap daily: close 1, 6 and open 5; lift helium trap out of its storage dewar and hold at room temperature for a few seconds; reinsert helium trap into dewar and close 5, open 1 and 6 (don't forget to re-close vent on storage dewar). A slow rise in base temperature and an increase in G2 likely indicate that the helium trap is becoming clogged and requires a quick clean.

Warming Up

- Close needle valve evacuate 1K pot. Close 1K pot pumping valve at top of insert.
- Close 13a and open 5 and 9, and make sure dumps valves are open. This sets the fridge in single shot mode, with the ^{3}He being extracted from the insert but not returned.
- Increase the power supplied to the still and mixing chamber heaters to maximum.
- Check that all the mixture has been returned to the dumps by reading G2 and comparing it to the value at the beginning of the cooldown (~525 mbar as of this writing, although G2 is not independent of atmospheric pressure and may vary by a

few percent).

- Once all the mixture is out of the insert and P1 < 0.1 mbar, close 1, 5, 6, 9, 12a and the dumps valves. Note that there is mixture left behind pump and up to valve 13a. Close all valves on fridge insert.
- Make sure all the valves on the cabinet and on the insert are closed, disconnect the piping and electrical leads to the insert, and remove the insert from the dewar. A small amount of He or air can be used to soften the IVC.
- Reconnect and monitor the diagnostic thermometry and wait until the insert has reached room temperature.
- To remove the IVC, fit the slide hammer ring over the IVC and bolt the plate to the underside of the large diameter part of the IVC. Vent the IVC by opening the IVC valve at the top of the insert. Support the IVC to prevent it from falling when the seal is broken, and slide the slide hammer ring down sharply against the plate. It may take a few impacts to free the IVC tube.
- If warming traps, pump on them through 5A, 2A, 7, 11a.

<u>Optional Throughput Test / Dilution Unit Leak Check Procedure (using external He supply)</u>

- All valves on cabinet panel should be closed, as well as still and condenser valves at top of insert.
- Attach leak detector directly to IVC pumping port at top of insert and monitor leak signal from IVC.
- If traps haven't been cleaned, clean them following procedure outlined in 'Condensing and Circulating Mixture' section above.
- Cool nitrogen trap by inserting it in its dewar. Cool helium trap by inserting it in a full

60 liter storage dewar.

- Attach a valved hose nipple to 'Vent 1' port at rear of cabinet and connect it to a UHP He gas supply with a thick flexible hose (the old Airco regulator and hose in the screen room work well).
- Pump out flexible hose through 5A and 2A; the overriding concern throughout is to prevent any air from getting into the dilution unit. Close 5A and 2A.
- Open 11a, 12a and 3.
- Pressurize still pipe to ~ 950 mbar on G1 by introducing UHP He through Vent 1, 7, 11a, traps, 12a, 3. To avoid damaging the traps, do not overpressure (set regulator ~ 3 psi) and close 7 periodically to allow He in traps to flow into still line. Be patient: this will take ~15 minutes.
- Close off hose nipple valve at cabinet and He supply.
- Close 12a.
- Evacuate traps through 11a, 7, 2A, 5A; after traps are empty, close 11a.
- Close 3 and pump out G1 gauge space through 2, 7, 2A, 5A until G1 = 0. G1 will be used to monitor throughput.
- Close 2 and 7.
- Open still valve at top of insert to let purified He into dilution unit.
- Open condenser valve at top of insert.
- Open 1 and record throughput rate by monitoring G1.
- Check leak detector for leak signal, which would indicate a leak from dilution unit to IVC.
- Typical throughput rates are ~50 mbar/minute at 300 K, ~300 mbar/minute at 77 K.
- Evacuate He from system by pumping through 1, 3, 2, 7, 2A, 5A. Pump until P1 reads less than ~ 3×10^{-2}.
- Close still and condenser valves at top of insert and close all valves on cabinet.
- Disconnect leak detector from IVC port and introduce He exchange gas into IVC.

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