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"Strain Sensing Field-Effect Transistors in Nano-Electromechanical Systems"

presented by Rex Gordon Beck

candidate for the degree of Doctor of Philosophy and hereby certify that it is worthy of acceptance.

Signature ....

Typed name Robert M. Westervelt, Chair

Signature ....

Typed name Michael Tinkham

Signature ....

Typed name Frans A. Spaepen

Date May 15, 1998

Strain Sensing Field-Effect Transistors in Nano-Electromechanical Systems

A thesis presented

by

Rex Gordon Beck Jr.

to

the Department of Physics
in partial fulfillment of the requirements
for the degree of
Doctor of Philosophy
in the subject of

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ABSTRACT

This thesis describes self-sensing cantilevers made from GaAs/AlGaAs heterostructures containing a two-dimensional electron gas (2DEG). The cantilevers have micron size lateral dimensions, nanometer size thicknesses, and deflection sensors composed of strain-sensing field-effect transistors (FETs) integrated into their base.

We fabricated strain sensing FETs from a GaAs/$Al_{0.3}Ga_{0.7}As$ heterostructure containing a 2DEG 520 Å beneath the surface. We measure FET noise corresponding to a gate charge noise < 0.2 electrons/√Hz. GaAs Field-effect transistors sense strain via the piezoelectric effect. We measured volume strain sensitivity 2 x 10^{-9}/√Hz at T = 4.2 K and 4 x 10^{-9}/√Hz at T = 77 K limited by FET noise. Such FETs with small size, low noise, high operating speed, and low power dissipation are ideal for integration into small GaAs/AlGaAs mechanical systems as strain sensors.

Three self-sensing cantilevers were demonstrated. The first, with dimensions 65 x 11.4 x 0.5 μm^3, showed the measurement of the cantilever resonance frequency 88.2 kHz using the strain sensing FET. The second, with dimensions 65 x 11.4 x 0.25 μm^3, was used as a scanning probe microscope cantilever at T = 4.2 K. Measured deflection noise 10 Å/√Hz at 100 Hz corresponded to a force noise 19 pN/√Hz at 100 Hz limited by FET 1/f noise. The third, a scanning probe microscope cantilever 3 x 2 x 0.129 μm^3, had a calculated spring constant 4.7 N/m and resonance frequency 11 MHz. The measured FET charge noise < 0.001 e/√Hz combined with the increased deflection sensitivity found in smaller cantilevers gives a projected deflection sensitivity of 0.002 Å/√Hz.

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CHAPTER 1

INTRODUCTION

Microelectromechanical systems (MEMS) provide a novel environment for studying new physical phenomenon, offer new ways to approach experiments in the laboratory, and open up many possibilities for device applications. Traditional uses for small electromechanical systems include strain-sensors, pressure sensors, and accelerometers for systems like airbags in cars. The past 10 years have witnessed the development of more and more uses for MEMS. A few examples include micro-electromechanical switches, atomic force microscope cantilevers, mirrors, interferometers, motors, electrometers, jet turbine engines and generators. The possible applications for such systems seem bounded only by the human imagination. These advances would not have been possible without processing technology that has been developed by the semiconductor industry in its quest for smaller, faster devices. These resulting techniques have greatly advanced the fabrication of two-dimensional electronic structures. To make mechanical structures, one simply needs a third dimension. One addition to the existing fabrication technology, the use of an underlying sacrificial layer

that can be selectively etched to free the structure above it, makes possible the fabrication of mechanical structures on the micron size scale.

Micro-electromechanical systems are attractive because of the advantages found in small mechanical systems. First, small structures enjoy nearly ideal mechanical properties. Such devices may have a perfect crystal structure with no dislocations, resulting in a structure that is strong and able to be strained with little dissipation. Mechanical resonators can be made from these single crystal structures having mechanical quality factors ~ 60,000 usually limited by surface effects [Albrect, (1991)]. Second, small systems generally have high resonant frequencies and thus can operate very fast. One could imagine mechanical switches that operate at speeds comparable to transistor cutoff frequencies or the incorporation of mechanical components in a microwave integrated circuit. Third, the spring constants for small systems are generally small. This allows fabrication of devices that can be actuated by very small forces and also makes possible the detection of small forces. The record for force detection is currently held by Stowe et al. (1997) where they report cantilevers with force noise levels ~ 3×10^{-18} N/$\sqrt{\text{Hz}}$. Finally, because these devices are made from semiconductors using many of the same process steps used for integrated circuit fabrication, they are ideally suited for on-chip integration into more complex electronic systems.

Most work in micro-electromechanical systems has been concerned with structures ranging in size from ~10 microns to ~1mm. At these size scales, fabrication is relatively easy and many useful devices can be made. Some groups [Cleland et al. (1998); Tighe et al. (1997)] are exploring mechanical systems having smaller sizes. Smaller sized systems have higher resonant frequencies (~ 10 MHz to ~ 10 GHz), smaller

spring constants, and make possible the detection of smaller forces or displacements. They can also be used to reach new physical regimes for experiments. For example, Tighe et al (1996) have constructed devices to study electron-phonon interactions in systems where phonon number is limited by device dimensions.

Generally, it becomes more difficult to sense forces or displacements as the device size becomes smaller. The sensor must be small, operate at high speeds, and ideally have the ability to be integrated into the mechanical structure of the device to eliminate alignment difficulties. Choices of available sensors fall into two broad categories: external deflection sensors and internal strain sensors. External sensors include optical beam bounce, interferometric, magnetic, capacitance, tunneling current, and thermal conductivity. Internal strain sensors include piezoresistive and piezoelectric. Excluding external sensors, due to the small size requirements and the difficulty of alignment, leaves the two integrated strain sensing effects, piezoresistive and piezoelectric, as the preferable candidates for sensors in small systems.

This object of this thesis is to fabricate, characterize, and demonstrate a strain sensor that can be integrated into nano-scale mechanical structures. We will make small mechanical structures from a GaAs/AlGaAs heterostructure containing a two-dimensional electron gas. We then integrate field-effect transistors into the mechanical structure of the devices to act as strain sensors. Field-effect transistors sense strain via the piezoelectric effect. GaAs/AlGaAs field-effect transistors are well suited for strain sensing in small mechanical systems for the following reasons. First, they can be integrated into the mechanical structure of the systems and thus open the possibility for making small or complex nano-electromechanical systems. Second, they can operate at

high speeds to match the high resonant frequencies in small systems; the cut-off frequency for some of our devices is calculated to be above 1 GHz, and commercial heterostructure FETs have cut-off frequencies up to 250 GHz [Chang, (1994)]. Third, they can be made with very low noise; we will demonstrate FETs that display a gate charge noise ~ 0.001 $e/\sqrt{Hz}$. Commercial GaAs/AlGaAs HEMTs are known for possessing the lowest noise figures at high frequencies [Chang, (1994)]. Finally, FETs can operate with low power dissipation. Because FETs provide power gain, they can operate with good sensitivity and low power dissipation. This becomes a crucial requirement when integrating these sensors onto small devices that can only dissipate small amounts of power due to their small size.

We will concentrate on a particular small mechanical system in this thesis: the GaAs/AlGaAs cantilever. We choose a cantilever as a model system to demonstrate the fabrication of a small mechanical system from a heterostructure and also to demonstrate the operation of an integrated FET as a strain sensor. This work will present three different cantilevers made with integrated FETs. The first will demonstrate the measurement of the mechanical resonance frequency of a cantilever using an FET. The second will demonstrate the use of a heterostructure cantilever as a low temperature scanning probe microscope cantilever. The third will demonstrate a smaller cantilever that realizes the advantages found in smaller levers: high resonant frequency and increased deflection and force sensitivity.

1.1 Overview of the thesis

Following this introduction, chapter two presents a model for field-effect transistor operation in the low field and high field regimes, and reviews the noise mechanisms in the FET both at low frequencies (1/f noise) and high frequencies, with a view to designing the lowest noise devices. The second part of Chapter two describes the mechanical characteristics and responses of cantilevers to both static and dynamic forces. This chapter ends with a discussion of cantilever noise sources in the context of the ultimate force sensitivity.

Chapter three describes the fabrication steps for field-effect transistors and for freestanding two-dimensional electron gas structures like cantilevers. It begins with a description of the heterostructure material and continues with a detailed description of the fabrication steps. Electron beam lithography was used for all the patterning steps. The field-effect transistor fabrication procedure is heavily based on earlier work in the group by Doug Mar [Mar, (1994b)]. Fabrication steps for three-dimensional structures are presented including etching, undercutting, drying, passivating, and scanning probe microscope cantilever tip deposition.

Chapter four describes the fabrication and characterization of strain-sensing field-effect transistors and reports on the measured charge noise of the device $< 0.2\ e/\sqrt{Hz}$ at $T = 10$ K. It also describes the experiments performed to measure FET strain sensitivity of $2 \times 10^{-9}/\sqrt{Hz}$ at 10 K and $4 \times 10^{-9}/\sqrt{Hz}$ at 77 K. A model of the FET strain response is presented comparing the effects of both the deformation potential and the piezoelectric effect. The piezoelectric effect is found to be able to account for the strain signal.

Chapter five describes the fabrication and operation of three cantilevers made from heterostructure materials and containing two-dimensional electron gases with integrated strain sensing FETs. The first device demonstrates the measurement of a cantilever mechanical resonance frequency using a strain sensing FET. The second cantilever with dimensions 65 μm x 11.4 μm x 0.25 μm was mounted in a low temperature scanning probe microscope and was used to image a sample at T =4.2 K. The third device is a smaller scanning probe microscope cantilever with dimensions 3 μm x 2 μm x 0.129 μm and represents a significant improvement in fabrication techniques. The on-cantilever FET characteristics are presented, and projected force and displacement sensitivities are given.

The final chapter summarizes the work and suggests some improvements to the FET and cantilever designs. It also suggests ideas for future experiments.

CHAPTER 2

THEORETICAL BACKGROUND

This chapter describes the operation of field-effect transistors and cantilevers. A model of field-effect transistor operation is presented for regimes both below and above the current saturation point. Transistor noise sources are discussed including intrinsic noise sources like 1/f and channel noise and extrinsic noise sources due to parasitic resistance. The second half of this chapter describes cantilever characteristics and discusses cantilever noise sources in the context of ultimate sensitivity limits.

2.1 Field-Effect Transistor Model

This section reviews a model for a two-dimensional electron gas (2DEG) field-effect transistor (FET). The FET discussed here consists of a channel containing a 2DEG through which electrons can flow from the source contact to the drain contact. A Schottky gate separates drain and source and thus modulates channel conductance. This section first briefly introduces heterostructures and 2DEGs and addresses the issue of determining the electron gas density in the FET channel. Expressions for drain current as a function of gate-source voltage and drain-source voltage for low drain-source voltages

are presented. Then it introduces the concept of velocity saturation and explores the high field operation of the FET in its current saturated state.

2.1.1 Density of electrons in the two-dimensional electron gas channel

The transistors described in this thesis are fabricated from GaAs/$Al_xGa_{1-x}As$ heterostructures. In these heterostructures the conduction band energy profile can be engineered because the conduction band energy varies with the aluminum concentration in $Al_xGa_{1-x}As$. A discussion of how these heterostructures are grown and how the 2DEG forms in them is given in section 3.1. Figure 2.1a shows one of the heterostructures used in this thesis. The layers composing this structure from the substrate to the surface include 5250 Å $Al_{0.3}Ga_{0.7}As$, 200 Å GaAs, 220 Å $Al_{0.3}Ga_{0.7}As$, Silicon delta doping layer $8 \times 10^{12}/cm^2$, 250 Å $Al_{0.3}Ga_{0.7}As$, 50 Å GaAs. The 2DEG is formed by electrons being thermally excited from the Si donors in the $Al_{0.3}Ga_{0.7}As$ layer and falling into the GaAs well. The potential profile caused by the GaAs well and the positively charged donors quantum mechanically confines the electrons to electronic subbands in the well. Here, electron motion is limited in the growth direction but free in the directions parallel to the interface. The energy of the electronic subband is given by a self-consistent solution of Poisson's and Schrodinger's equations.

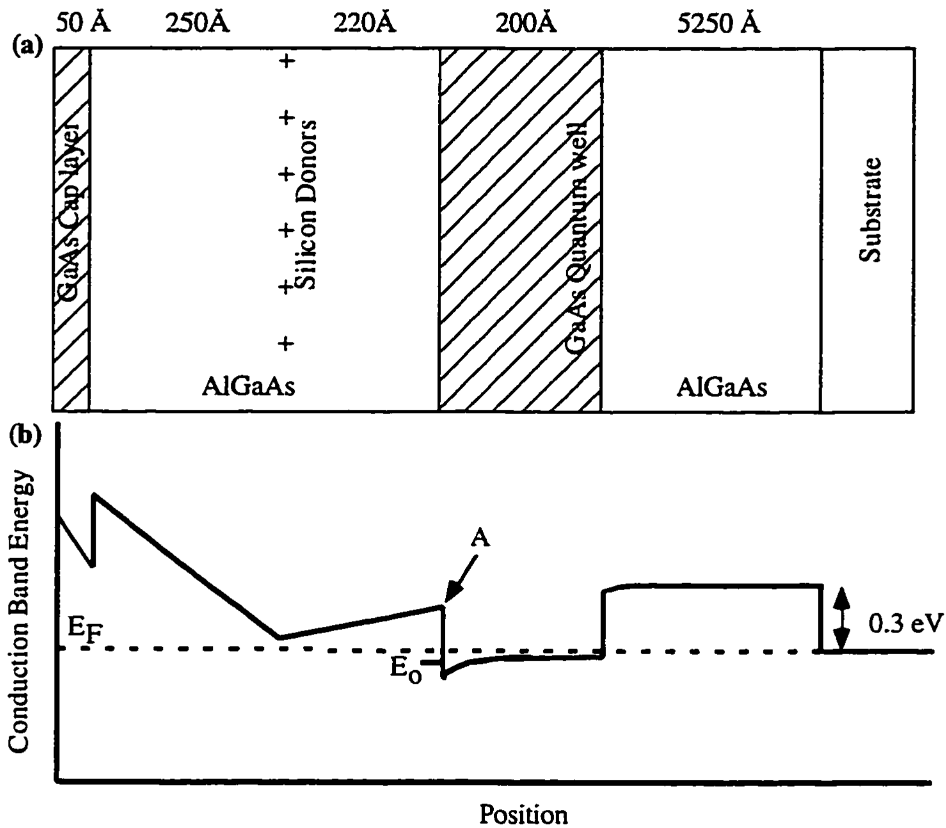


Figure 2.1 (a) Diagram showing epitaxial layer structure for wafers used to make field-effect transistors. Clear regions are $Al_{0.3}Ga_{0.7}As$, diagonal lined regions are GaAs, and the plus signs indicate silicon donors. The delta doping concentration is $\delta = 8 \times 10^{12}/cm^2$ (b) The resulting conduction band profile. The dotted line indicates the Fermi Energy and E_o represents the energy of the first subband.

The number density of electrons in the well can be calculated in the following way. The density of states D for a 2DEG layer is independent of energy and is given by $D = m^*/\pi\hbar^2$ where m* is the electronic effective mass, and $\hbar$ is Planck's constant divided by 2π. In GaAs m* equals 0.067m where m is the rest mass of the electron. D is an expression for the density of states in each subband. Assuming only the first subband, having energy E_o, is occupied we can write the electron density n_s following Delagebeaudeuf et al. (1982)

$$n_s = Dk_BT\ln\left(1+\exp\left(\frac{(E_o - E_F)}{k_BT}\right)\right) \qquad (2.1)$$

where k_B is Boltzmann's constant, T is the temperature, and E_F is the Fermi energy. Equation 2.1 reduces to $n_s = D(E_F - E_0)$ at the low temperatures of interest in our experiments.

2.1.2 Charge Control

The electronic number density in the FET channel is modulated by the voltage applied to the Schottky gate; because the density is linearly related to the Fermi level, we can also think of the gate as modulating the local Fermi level. Here we have the simple relation between electron sheet density and gate voltage V_G, $n_s = (\varepsilon/eh)(V_G - V_{off})$ where V_{off} is the voltage on the gate that annihilates the 2DEG, ε is the permittivity of the layer between gate and channel, and h is the distance between the gate and 2DEG. More realistic models account for the finite thickness of the 2DEG by replacing h with $h + \Delta h(x)$ where $\Delta h(x)$ is the width of the 2DEG [Drummond et al. (1982)]. During normal FET operation the electron density in the channel $n_s(x)$ and therefore the width of the 2DEG $\Delta h(x)$ are not constant throughout the length of the channel. Electronic sheet density at position x depends on the channel voltage at that position $V_c(x)$ and can be expressed as

$$n_s(x) = (\varepsilon/eh)(V_G - V_c(x) - V_{off}). \qquad (2.2)$$

2.1.3 Calculation of Drain Current

The drain current at any point in the channel is given by $I_D = en_s(x)Zv(x)$ where $n_s(x)$ is the sheet density at position x, Z is the channel width and v(x) is the electron velocity at position x. For fields less than some critical field E_c the electron velocity is linearly proportional to the field $v(x) = \mu\, E(x)$ where μ is the electron mobility and $E(x) = dV_c(x)/dx$. Thus we can write the drain current as [Delagebeaudeuf et al. (1982)]

$$I_D = \mu Z \frac{\varepsilon}{h}(V_G - V_c(x) - V_{off})\frac{dV_c(x)}{dx} \qquad (2.3)$$

Assuming that the current is constant throughout the channel we integrate equation 2.3. For small drain voltages where the current is linearly proportional to the applied voltage we integrate 2.3 over the length L_c of the channel

$$I_D = \mu Z \frac{\varepsilon}{hL_c}\left(V_G - V_{off}\right)\left(V_c(L) - V_c(0)\right). \qquad (2.4)$$

This expression demonstrates that at small drain-source voltages the FET acts as a voltage controlled resistor. Including the effects of drain and source access resistances, r_D and r_S respectively, gives

$$\frac{V_D}{I_D} = r_S + r_D + \frac{L_c h}{\mu Z \varepsilon (V_G - V_{off})}. \qquad (2.5)$$

At higher drain-source voltages a model is used involving the concept of velocity saturation. According to this model, at low fields electron velocity is proportional to the electric field $v_e = \mu E$ where μ is the mobility. However, at fields above some critical field E_c, the electron velocity saturates and becomes independent of electric field $v_e = \mu E_c = v_s$. In GaAs this saturation velocity is measured to be around 2×10^7 cm/s. Velocity saturation can be motivated by noticing that optical phonons provide some upper bound to electron velocity; in GaAs optical phonons have an energy about 5 meV and a dispersion curve that is fairly flat. It becomes very favorable for an electron to scatter into a lower energy state once the electron acquires enough energy to scatter by emitting an optical phonon. This velocity saturation effect is the cause for the current saturation in field-effect transistor characteristics. It should be emphasized that this is only a model. The actual behavior of non-equilibrium electrons in GaAs is quite complex. For example, the effective velocity of electrons actually surpasses the saturation value at electric fields *lower* than the critical field E_c. This velocity then decreases with increasing field to its saturated value at $E = E_c$ [Grubin, (1990)]. Also, there is a finite energy relaxation time. If an electron can traverse the channel in a time shorter than this energy relaxation time, then it can travel with velocities much greater than its saturation velocity while it is in the channel [Shur, (1989)]. This behavior has some consequence for designing transistors with submicron gate lengths. In spite of all these complications the velocity saturation model still gives a reasonable picture of how transistors work and will be useful for understanding their noise mechanisms.

In order to calculate the saturation current we need to determine the drain current which causes the electric field in some part of the channel to be equal to the critical field $E_c = v_s/\mu$. The field in the channel, calculated using equation (2.3), is not uniform throughout the channel but rather has a maximum value at the drain side. When this drain side electric field equals the critical field, the electrons become velocity saturated there and the drain current saturates. The saturation current I_S at which the drain side electric field reaches the critical field is given by [Delagebeaudeuf et al. (1982)]

$$I_S = \frac{\mu Z \varepsilon}{2hL_c}\left(V_G - V_{off} - r_s I_s\right)^2 \tag{2.6}$$

for long gate length devices. For transistors with short gate lengths the saturation drain current acquires a linear relationship to the gate voltage

$$I_S = \frac{v_s Z \varepsilon}{h}\left(V_G - V_{off} - r_s I_s - E_c L_c\right) \tag{2.7}$$

where E_c is the critical field.

2.1.4 High Field Operation

The above description of FET operation was for low values of the electric field in the channel; the maximum electric field in the channel was either less than or equal to the critical field E_c. We explore here the model for the high field regime. This model is

helpful in gaining insight into the FET operation and also for understanding channel noise sources in the saturation regime.

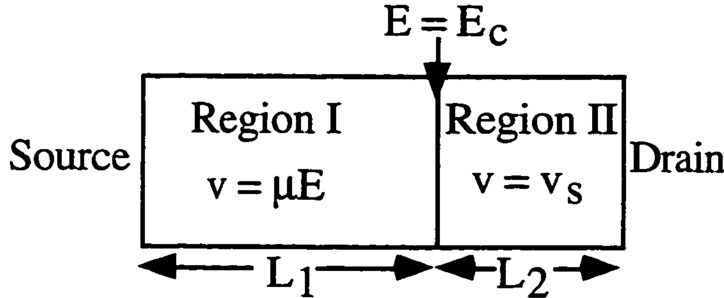


Figure 2. 2 Schematic showing the two regions in the FET channel that develop when the current is saturated. Electrons in region I obey Ohm's law while electron velocity in region II is independent of electric field.

In the saturation region the FET channel can be divided into two regions as shown in Figure 2.2. The electron velocity is saturated in region II and linearly proportional to E in region I. Region II develops first at the drain side of the channel where the electric field is the highest and has a boundary with region I defined as the location where $E(x) = E_c$. The drain current I_D can be calculated using this model and considering region II. Current through region II is given by the product of the number of charge carriers and their saturated velocity v_s [Brookes (1986)]

$$I_D = n_s(L_1)Zv_s = \frac{Z\varepsilon}{(h+\Delta h)} V_{off}\, p v_s \qquad (2.8)$$

where $n_s(L_1)$ is the charge density at L_1 and for the entire region II, v_s is the saturation velocity, and p is the reduced potential $p = (V_G - V_{off} - V_c(L_1))/V_{off}$. The length of region I is given by Brookes as

$$L_1 = \frac{\left(s^2 - p^2\right)}{2p}\frac{V_{off}}{E_s} \tag{2.9}$$

Where $s = (V_G - V_{off})/V_{off}$.

Calculation of the drain-source voltage V_{DS} is more complicated but can be found by integrating the potential in the ohmic and non-ohmic regions. The potential drop in region I is simply given by $V_{off}(s - p)$ while the potential in region II is determined by a solution of Poisson's equation satisfying the boundary conditions given by the drain and gate potentials. The resulting total drain-source voltage is then given by [Brookes, (1986)]

$$V_{DS} = V_{off}\left(s - p + \frac{2(h + \Delta h)}{\pi L}\left(\frac{E_s L_c}{V_{off}}\right)\sinh\left(\frac{\pi L_2}{2(h + \Delta h)}\right)\right) \tag{2.10}$$

where $L_c = L_1 + L_2$. From the above model, one can obtain expressions for parameters describing the FET like transconductance $g_m = -dI_D/dV_{GS}$ and small signal drain source resistance $r_{ds} = -dV_{DS}/dI_D$.

A simplified expression for the transconductance can be derived by differentiating the saturation current expression for the long gate FET given in the low field section, Equation (2.6). This results in $g_m = 2\sqrt{\frac{\mu Z \varepsilon}{2dL_c}}\sqrt{I_S}$,which generally describes the behavior of the transconductance that we measure.

2.2 Noise

The noise associated with any electrical device can be classified into two regimes based on how the noise power varies with frequency. At low frequencies the noise power generally decreases with some power of the frequency while at higher frequency the noise is constant or white. This section will address the source of noise in both of these regimes in the context of field-effect transistor operation.

2.2.1 Low Frequency Noise

At low frequencies many systems exhibit "generic" 1/f noise defined as noise power that is inversely proportional to some power α of the frequency $1/f^{\alpha}$ where $0.8 < \alpha < 1.4$. Noise having this behavior is ubiquitous; it has been seen in diverse electrical systems such as resistors and even in various physiological phenomenon like the frequency of word usage verses the length of words (Zipf's law) [Bell, (1985)]. In spite of much effort, especially in the early 1980's, no fundamental source for this noise has been found [Weissman (1988)]. In semiconductors, however, it is generally agreed that the origin of this type of noise is charge trapping and detrapping [Weissman, (1988)].

Generally, a 1/f noise power spectrum can be derived from any process having some characteristic time. For example, consider the situation where some random event can affect the sample resistance. The probability that this even is still "on" after a given time t is given by $p = p_0 e^{-(t/\tau)}$. Using a Fourier transform to find the spectrum of p yields a Debye-Lorentzian distribution $P(\omega) \propto \tau/(1+\omega^2\tau^2)$. A noise spectrum $s(\omega)$ is composed of

the added effects of many of these events having some distribution of characteristic times $D(\tau)$;

$$s(\omega) \propto \int \frac{\tau}{1+\omega^2\tau^2} D(\tau) d\tau. \tag{2.11}$$

If $D(\tau) \propto 1/\tau$ for $\tau_1 < \tau < \tau_2$ then $s(\omega) \propto 1/\omega$ for $1/\tau_2 < \omega < 1/\tau_1$ and we have a model producing 1/f noise.

McWhorter (1957) proposed a physical model of 1/f noise involving traps in a semiconductor/oxide interface. Characteristic times for these traps would have the form $\tau = \tau_o \exp(L/Lo)$ where L is the distance from the trap to the carriers. For this case $D(\tau) \propto D(L)(dL/d\tau) \propto D(L)/\tau$ where D(L) is the distribution of the distances between the traps and the carriers. Thus, if the traps are uniformly distributed in space then 1/f noise can be accounted for. In practice, these traps must also have a uniform energy distribution. This arises from the weak temperature dependence of 1/f noise in semiconductors. If only those traps close to the Fermi level display much switching, then as the temperature changes there must be a relatively constant number of traps close to the Fermi level. Thus, a realistic model demands a uniform distribution of traps both in position and in energy [Weissman, (1988)].

More generally, but following the McWhorter model, Dutta and Horn [Weissman (1987); Dutta et al. (1981)] have shown that 1/f noise can be generated from any thermally activated process with a fairly flat distribution. If the characteristic rate τ is thermally activated then $\tau = \tau_o \exp(E/k_B T)$ and $D(\tau) \propto D(E)\,(dE/d\tau) \propto D(E)/\tau$ and the problem for justifying 1/f noise becomes that of finding some physical situation where

there is an even distribution D(E) in the energy range $k_BT\ln(\tau_1/\tau_0) < E < k_BT\ln(\tau_2/\tau_0)$. Physically this can be accounted for by a number of pairs of traps exchanging electrons where the activation energies between the traps have a slowly varying distribution over some energy range $E \sim k_BT$. In our systems this situation may arise from traps in the non-conducting region (AlGaAs) exchanging electrons in a way that affects the sample resistance. An experiment by Ralls et al. (1984) demonstrated the effect of a single switching event on the resistance of a narrow Si inversion layer. Later Rogers et al. (1984) studied small MIM tunnel junctions and showed the evolution of several switchers with Lorentzian spectra into a 1/f spectrum at higher temperatures.

An empirical formula by Hooge (1981) states that noise power $S_R(f)$ of a sample with resistance R is inversely proportional to the number of charge carriers N_c and the frequency f

$$\frac{S_R(f)}{R^2} = \frac{\alpha_H}{N_c f} \tag{2.12}$$

where α_H is a sample-dependent constant. This formula, although having no fundamental significance, provides a useful rule of thumb for estimating $S_R(f)$ in many materials. It also implies another characteristic of 1/f noise: larger samples having more carriers will display lower 1/f noise values. This result is also true for larger samples that have a corresponding increase in switching sites. For two dimensional resistors the noise should scale as $S_R(f) \propto 1/A$ which is consistent with any resistance fluctuation model where a fluctuation is localized and thus will only affect a small region independent of total resistor area [Rogers et al. (1984)].

Noise in modulation doped GaAs/AlGaAs field-effect transistors has also been investigated by several groups [Loreck et al. (1983); Duh et al. (1983)]. Loreck et al. suggest that the source for 1/f noise is traps in the AlGaAs layer and have measured their activation energies. Duh et al. have reduced the effects of these traps on channel conductance by doping the AlGaAs layer and screening the effect. Thus 1/f noise could be reduced by reducing the number of traps in the AlGaAs layer or by screening it by an additional doping layer. The latter will degrade electron mobility and therefore is not desirable.

Independent of the source of 1/f noise, the magnitude of the resistance noise spectrum $S_R(f)$ will decrease with channel length L_c and width Z; $S_R(f) \propto 1/L_cZ$ [Van Der Ziel, (1976); Klassen, (1971)]. Gate voltage noise is also proportional to $1/\sqrt{A}$ where A is the area of the transistor gate. This behavior is important in designing low noise devices. In this design, the ratio of noise to signal $v_{ng}/\Delta V_{GS}$ where v_{ng} is the voltage noise on the gate and ΔV_{GS} is the signal should be minimized for best performance. For low impedance sources, where ΔV_{GS} is independent of gate area, $v_{gn}/\Delta V_{GS} \propto 1/\sqrt{A}$ and it is beneficial to have FETs with large areas and low 1/f gate voltage noise. However, when measuring a limited amount of charge, which is the case for high impedance sources, $v_{gn}/\Delta V_{GS} \propto (1/\sqrt{A})/(Q/A) = \sqrt{A}/Q$ where Q is the charge signal on the gate. This result indicates that best signal to noise is achieved with a small gate area. This example illustrates the trade-off between decreasing the gate voltage noise by using a larger area gate but suffering a corresponding increase in gate current noise.

2.2.2 High Frequency FET Noise

At low frequencies, as was shown above, transistor noise is dominated by switching events that cause noise with a characteristic 1/f power spectrum. At higher frequencies other fundamental noise sources dominate, namely Johnson and shot noise, both of which have magnitudes independent of frequency. Models incorporating these noise sources in the FET gate and channel give good agreement with measured noise performance in GaAs MESFETs [Hewitt, (1976)]. These models predict a noise figure that rises linearly with frequency.

Before enumerating the various FET noise sources, we review two fundamental noise sources prominent at high frequency: Johnson or Nyquist noise and shot noise. Johnson noise is an equilibrium fluctuation in the voltage across a resistor. It is white, or independent of frequency, and has a magnitude given by $\delta v_J = \sqrt{4k_B TR\Delta B}$ where k_B is Boltzmann's constant, T is the electron temperature, R is the resistance of the sample and ΔB is the bandwidth. This expression can be derived by considering a lossless transmission line with characteristic impedance R terminated at both ends by resistors of resistance R. In thermal equilibrium, the photons occupying the modes of this transmission line will dissipate power in the resistors corresponding to the noise voltage given above [Kittel, (1980)]. This noise is white up to frequencies where the photon energy, $\hbar\omega \sim k_B T$. Shot noise arises due to the discrete nature of charge and is associated with current flow over a barrier. If the electron motion is uncorrelated it will have a magnitude $i_{shot} = \sqrt{2e\Delta BI_{dc}}$ that is independent of frequency up to frequencies

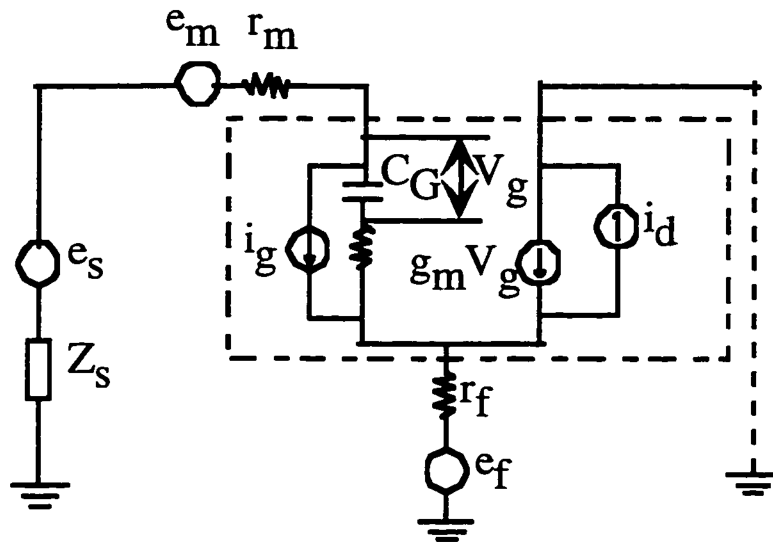


Figure 2. 3 FET noise model after Pucel et al.. The dotted box outlines the intrinsic FET and its noise sources. Also shown are the parasitic resistances r_f and r_m that contribute to the device noise. The FET is measuring a sample with impedance Z_s and resistance that produces Johnson noise with magnitude e_s.

where the electron motion is correlated and the noise power spectrum falls as $1/f^2$ [Bell, (1960)].

Figure 2.3 shows a circuit model after Pucel et al. (1975) incorporating high frequency noise sources for the FET. The area enclosed within the dashed box represents the intrinsic FET. The conventional FET operation is modeled by the signal voltage V_G placed across the gate-to-source capacitance C_G in series with the gate-to-channel resistance R_i producing a current $g_m V_g$ in the channel. Two noise sources are included in the intrinsic FET: the channel current noise i_d and the gate noise current i_g. When the FET channel is not biased the channel current noise i_d simply equals the Johnson noise current due to the resistance R_{DS} of the channel $i_d = \delta v_J / R_{DS}$. When the channel is biased, i_d will increase beyond the Johnson noise value. Noise voltages generated in the channel will induce a change in electron density in the channel and a corresponding change in electron

number on the gate. Thus, a gate noise current i_g shown in Figure 2.2 is produced in response to this noise voltage in the channel. Because both the channel and gate noise currents are caused by the same noise voltages, they are correlated. Outside the box are the additional noise sources due to the parasitic resistances from the gate metallization layer r_m and the source access resistance r_f that produce Johnson noise voltages e_m and e_s respectively. Finally, the diagram includes the signal source, a sample with impedance Z_s, that produces Johnson noise e_s due to its resistance.

The extrinsic noise of this FET, defined as the noise due to the parasitic resistances, can be described by the Johnson noise voltages from the parasitic gate metallization and source access resistances. The intrinsic FET noise, represented by i_g and i_d, is produced by voltage fluctuations in the channel. The measured magnitude of the channel noise is higher than the one predicted by Johnson Noise given the resistance of the channel and temperature of the lattice. Although the exact sources comprising this additional noise are difficult to experimentally measure because they are difficult to isolate, some noise contributions can be modeled. Specifically the following four sources may account for the increased noise in the FET channel [Liechti, (1976);Brookes, (1986)].

First, a Johnson noise voltage fluctuation in region I of Figure 2.2, where the electrons obey Ohm's law, is amplified and results in a drain-source voltage noise greater than the Johnson noise magnitude. This can be seen from the following argument, which assumes a constant channel current. A fluctuation in the channel voltage at a position in region I will cause a change in electron density at that position. In order to keep the current constant, a change in voltage will occur at the pinchoff point, which is equivalent

to a change in the boundary position between region I and region II. This change in position is the amplification of the noise voltage [Pucel et al. (1974); Brookes, (1986); Ando et al. (1990)]. This effect can also be motivated if one imagines keeping a constant drain current by varying the drain source voltage in response to a charge placed in region I.

Second, the electrons in region I are being accelerated above the Fermi velocity by the electric field, an effect that is especially important for high mobility devices. This results in an electron temperature significantly higher than room temperature and increases Johnson noise. Third, high energy electrons will scatter more easily. The scattering may be into different subbands in the quantum well, into the AlGaAs layer, or into another valley in GaAs. In any case, this process will scatter electrons into regions where mobility is decreased causing a further increase in the Johnson noise [Klaasen, (1970); Baechtold, (1972); Aninkevicius et al. (1992)].

The fourth source of noise originates from region II of Figure 2.2. Here, electron velocity is saturated making electron motion independent of electric field. In this non-ohmic region the Johnson noise formula, which is valid in equilibrium, no longer describes the noise. Here the noise is characterized as high-field diffusion noise and will have a mean squared current noise $S_i(x)$ proportional to the high-field diffusion constant D_n.

$$S_i(x) = \frac{4e^2 D_n n_s(x) A \Delta B}{\Delta x} \qquad (2.13)$$

where A is the effective cross-sectional area of the saturation region and Δx is a small length of the channel about point x. This expression reduces to the familiar Johnson noise formula using the Einstein relation $qD_n = kT\mu$, which is valid at equilibrium. Noise in this region can be viewed as the formation and transport of dipole layers by a voltage fluctuation at one end of region II [Statz et al. (1974)].

A figure of merit describing FET noise is the noise figure NF. The noise figure is a dimensionless parameter given by

$$NF = \frac{\text{Noise power output of FET and sample}}{\text{Noise power output due to sample thermal noise}} \qquad (2.14)$$

where the numerator includes the output noise power from both the sample and the FET while the denominator includes only the noise power of the sample (assuming the FET is a noiseless amplifier).

Pucel et al. (1975) calculated the noise figure for the circuit shown in Figure 2.2 by considering the noise current contribution of all the sources shown to the short-circuited drain-source noise current. They express this figure in terms of a power series involving frequency and some parameters describing the intrinsic noise sources [Pucel, et al. (1975)]. Including only the lowest order term of this series gives

$$NF \approx 1 + \left(\frac{fC_G}{\pi g_m}\right)\left(K_g\left[K_r + g_m\left(r_m + r_f\right)\right]\right)^{1/2} \qquad (2.15)$$

K_g and K_r are parameters describing the intrinsic noise sources.

The dominant source of noise, intrinsic or extrinsic, can be determined by measuring the noise dependence on drain current and drain-source voltage while the transistor is in the saturation regime. The magnitude of noise from intrinsic sources will vary with operating point while extrinsic sources will show little dependence on operating point. In practice, for most low noise transistors, the dominant noise source is the gate metallization resistance and the source access resistance. In our devices we notice little dependence of noise magnitude on operating point and therefore suggest that the noise is not dominated by intrinsic channel noise.

Fukui et al. (1978) have proposed an empirical noise figure, which will be denoted NF_o, that possesses a similar form to (2.15) but neglects the intrinsic channel noise contribution

$$NF_o = 1 + K_1 L_c f \sqrt{g_m (r_m + r_f)}\,. \tag{2.16}$$

where K_1 is an empirically determined parameter. This expression can be motivated by the more rigorous (2.15). First, we set the gate noise current due to intrinsic noise sources equal to zero then $K_r = 0$ and $K_g = 1$ in equation (2.15). We then use the relation for the cut-off frequency f_t of the FET given by $f_t = g_m/2\pi C_G \propto 1/L_c$, and we produce equation (2.16) by Fukui. For typical FETs Fukui et al. have found that $K_1 \sim 0.25$ sec for L_c expressed in microns.

From the above noise treatments we can select the optimum FET design for low noise measurements both at low and high frequencies. At higher frequencies where the dominant noise contribution comes from the parasitic resistances, it is desirable to

decrease these resistances. The gate metallization resistance can be decreased by making the gate thicker or by making one gate with multiple fingers to preserve gate width while decreasing resistance. Source access resistance can be decreased by placing the AuNiGe source contacts as close as possible to the channel. With our alignment capabilities this distance can be sub-micron.

2.3 Cantilevers

This section reviews some characteristics of cantilevers with a view to allowing the interested reader to optimize a cantilever for a specific application. It begins with general cantilever characteristics, continues by describing the static and dynamic response of the lever, emphasizing strain values, and finally ends with a discussion of cantilever noise sources including thermal noise limited measurements.

2.3.1 General Characteristics

A cantilever with thickness t, width w and length L enacted upon by a force F(z) that is perpendicular to the undeflected length of the cantilever will have a deflection u(z) that obeys the following differential equation [Chen, (1993)]

$$EM\frac{d^4u(z)}{dz^4} = -F(z) \qquad (2.17)$$

where E is Young's modulus of the cantilever material and M is the moment of inertia of the cantilever cross section. A force applied to the end of the lever $F(z) = F_o\delta(L - z)$ will result in a cantilever deflection of the form

$$u(z) = \frac{F_o}{EM}\left(\frac{1}{6}z^3 - \frac{1}{2}Lz^2\right). \qquad (2.18)$$

For a cantilever with rectangular cross section $M = (1/12)wt^3$. This information allows us to calculate the spring constant k of the cantilever

$$k = \frac{F_o}{u(L)} = \frac{Et^3w}{4L^3}. \qquad (2.19)$$

Equation (2.17) also allows us to determine the shape of a vibrating cantilever beam. For a cantilever beam driven with a sinusoidal vibration

$$u(z,t) = u(z)\cos(\omega t + \delta) \qquad (2.20)$$

Newton's second law gives the force distribution

$$F(z) = -\rho S\frac{d^2u(z,t)}{d^2t} = \rho S\omega^2u(z) \qquad (2.21)$$

where ρ is the cantilever mass density and S its cross sectional area. Equations (2.17) and (2.21), when combined, have a general solution of the form

$$u(z) = A\cos(\kappa z) + B\sin(\kappa z) + C\cosh(\kappa z) + D\sinh(\kappa z) \qquad (2.22)$$

where $\kappa = \frac{\omega^2 \rho S}{EM}$.

Solving this equation using the boundary conditions of zero force and moment at the cantilever end and zero deflection and slope at the cantilever base gives an expression for the resonance frequencies of the lever. The lowest mode will vibrate at a frequency f_{res} [Chen, (1993)]

$$f_{res} = \frac{0.56}{L^2}\sqrt{\frac{EM}{\rho S}}. \qquad (2.23)$$

For GaAs the mass density is $\rho = 5315$ kg/m^3 and for cantilevers with the length along the 011 direction E = 1.2 x 10^{11} N/m^2 [Cottam et al. (1973)]. Thus, for GaAs cantilevers with rectangular cross sections f_{res} can be written as

$$f_{res} = 771\frac{t}{L^2} \qquad (2.24)$$

with t and L in meters. It is interesting that this expression is independent of the cantilever width due to the linear dependence on width of *both* the spring constant and mass.

For a beam clamped at both ends the resonance frequency increases by more than a factor of 6 [Landau and Lifshitz, (1986)]

$$f_{res} = \frac{3.57}{L^2}\sqrt{\frac{EM}{\rho S}} = 4890\frac{t}{L^2} \qquad (2.25)$$

where the far right expression assumes a GaAs beam with a rectangular cross section with t and L expressed in meters.

2.3.2 Cantilever Response

Because we intend to sense the deflection of this cantilever with a strain sensor, we would like to know the strain produced by a given force. A static deflection produced by a force applied to the end of the cantilever results in a uniaxial strain field in the cantilever given by

$$\varepsilon(x,z) = x\frac{\partial^2 u(z)}{\partial z^2} = x\frac{F_o}{EM}(z-L) \qquad (2.26)$$

where x is the distance from the center of the cantilever in the plane of bending and z is the distance from the cantilever base. The maximum strain occurs at $z = 0$ and $x = t/2$. Here

$$\varepsilon_{\max} = \frac{6F_0L}{Ewt^2} = \frac{3t}{2L^2}u(L) \qquad (2.27)$$

is the maximum strain produced by a force F_o corresponding to a deflection of the end of the lever of u(L).

Dynamic response of the cantilever at frequency f is given by its complex force-to-deflection transfer function

$$h(f) = \frac{f_o^2 / k}{(f_o^2 - f^2) + i(ff_o / Q)} \tag{2.28}$$

where f_o is the resonant frequency and Q is the quality factor of the cantilever. One can use this to determine the spectral response of a cantilever R(f), which has units of m^2/Hz due to a driving force having the spectrum D(f), which has units of N^2/Hz [Albrect et al. (1991)]:

$$R(f) = |h(f)|^2 D(f). \tag{2.29}$$

From this equation we can see the advantage of exciting the cantilever at its resonance frequency; at resonance the rms amplitude of the response is a factor of Q larger than the static response.

2.3.3 Cantilever Noise Sources

Noise limits the ultimate sensitivity of cantilevers for force or displacement detection. In our systems there are three main sources of noise: 1) the noise from the

external measurement electronics, 2) the noise of the strain-sensing FET itself, and 3) the intrinsic noise of the cantilever due to thermal fluctuations.

The external measurement electronics have very low noise. We have used two configurations to measure the FET response, one using a PAR 113 voltage amplifier to measure the drain-source voltage and the other using an Ithaco 1211 current amplifier to measure the drain current. The PAR 113 has a noise temperature less than 10 K for frequencies between 10 Hz and 10 kHz and for the source resistances ~ 1 MΩ that it typically sees when it is used to measure drain-source voltage. The Ithaco exhibits current noise as low as 0.1 pA/√Hz for source impedance of 4 MΩ or 1 pA/√Hz for a source impedance of 35 kΩ. The latter value is closer to typical resistances seen by the Ithaco when it is connected to the drain. In most cases the FET noise dominates over both the external amplifier noise and the thermal noise of the cantilever.

If the FET noise could be reduced further, the ultimate limit to cantilever sensitivity would be imposed by the thermal noise of the cantilever. Thermal noise can be described by considering the cantilever in thermal equilibrium with a reservoir at temperature T. The equipartition theorem indicates that the potential energy in the cantilever will be $k_BT/2$. Setting this equal to $kx_{rms}^2/2$ where k is the cantilever spring constant and x_{rms} is the rms displacement of the cantilever end due to thermal noise gives the noise displacement amplitude. This displacement noise is caused by the cantilever being driven by a thermal noise force, denoted by S_F with units of N^2/Hz, which is considered to be independent of frequency. The integral of this thermal force noise multiplied by the magnitude of the transfer function 2.28 composes the thermal deflection x_{rms}^2

$$x_{rms}^2 = \int_0^\infty |h(f)|^2 S_F df. \tag{2.30}$$

In order to calculate the ultimate force sensitivity limited by thermal noise, we follow a calculation made by Stowe et al. (1997). First we solve (2.30) for S_F by performing the integral assuming Q >> 1

$$S_F^{1/2} = \left(\frac{2}{\pi Q f_o}\right)^{1/2} kx_{rms} = \left(\frac{2kk_BT}{\pi Q f_o}\right)^{1/2} \tag{2.31}$$

For a rectangular cantilever the factor $\frac{k}{f_o} = 1.56\frac{t^2 w}{L}\sqrt{E\rho}$. Thus for a given bandwidth ΔB the thermally noise limited minimum detectable force F_{min} for a cantilever with rectangular cross section is

$$F_{\min} = S_F^{1/2}\Delta B^{1/2} \approx (E\rho)^{1/4}(k_BT\Delta B)^{1/2}\left(\frac{wt^2}{LQ}\right)^{1/2} \tag{2.32}$$

This expression indicates that for thermally limited force measurements thin, narrow, and long cantilevers with high Q will have the best force sensitivity.

In practice, our low frequency (< 10 kHz) cantilever noise measurements are still limited by the 1/f noise of the strain sensing field-effect transistor. For the cantilever we fabricated with dimensions 65 x 11.4 x 0.5 μm^3 and a measured Q of 360 the thermally

limited minimum detectable force from equation (2.32) is $F_{min} = 4.1 \times 10^{-16} N/\sqrt{Hz}$. This number is 2 orders of magnitude above the smallest force measured with a cantilever [Stowe et al. (1998)] and about 5 orders of magnitude smaller than our best force resolution (~ 19 $pN/\sqrt{Hz}$) limited by the 1/f noise of the FET. If we can 1)make higher frequency measurements where we operate beyond the 1/f noise corner and 2) fabricate a low high-frequency noise FET the system may be able to reach its ultimate force sensitivity limited by cantilever thermal fluctuations.

CHAPTER 3

FABRICATION TECHNIQUES

This chapter describes the steps used for fabricating field-effect transistors and self-sensing cantilevers. Because this thesis presents different devices sharing many common fabrication steps, only the individual process steps are described here. When a device is introduced in later chapters, a brief description of fabrication is given that refers to the steps described in detail below. The processes covered in this chapter include: design and selection of the wafer material, cleaving and preparing sample chips from wafers, spinning of electron beam resists, electron beam lithography, thin film deposition techniques for both ohmic and Schottky contacts, three different methods for etching: ion milling, reactive ion etching and citric acid/hydrogen peroxide etching, passivation using self-assembled monolayers, electron beam deposition of scanning probe microscope tips, and release of mechanical structures by critical point drying.

Fabrication work can be done entirely with the facilities at Harvard, and mostly in Gordon McKay Labs. The scanning electron microscope facility is located on the first floor of Gordon McKay and maintained by Yuan Lu. The Gordon McKay cleanroom facility is located on the second floor and maintained by Steve Shepherd. Spinning of resists is performed in the inner clean room facility that is rated at class 100 while etching, thin film deposition, profilometry, and wirebonding are performed in the Class 10,000 outer clean room. The critical point dryer is located in the SEM sample preparation lab of

the Museum of Comparative Zoology.

3.1 Wafer Material

The devices described in this thesis were fabricated from semiconductor wafers composed of epitaxial layers of GaAs, $Al_{0.3}Ga_{0.7}As$ and AlAs grown on a GaAs substrate by molecular beam epitaxy (MBE). An epitaxial layer implies that its lattice sites are matched, one for one, with the underlying layer structure leaving no (in practice few) dislocations and resulting in a multi-layered, single crystal structure. A dislocation becomes energetically favored in an epitaxial layer of lattice spacing c and lattice mismatch Δc with it's underlying layer when the layer thickness approaches the limit $c^2/\Delta c$ [Gossard, private communication]. Because the lattice constants for GaAs and AlAs differ by less than 0.2 % [Adachi, (1987)], it is possible to grow relatively thick epitaxial layers, up to ~ 1 μm, in these systems without introducing a dislocation. In practice, however, there are defects inherent in the growth process. Defect densities in one atomic layer range from 100-1000 defects/cm^2 [Gossard, private communication]. For small devices, this density provides a reasonable probability that the crystal structure is perfect in the active area. Devices fabricated from perfect crystals possess high electron mobilities due to the lack of scattering from crystal imperfections and also enable the fabrication of high strength and low loss mechanical structures.

The technology used to grow these crystals is foundational to the work in this thesis. Wafer growth takes place in a molecular beam epitaxy (MBE) chamber. In this UHV chamber a wafer of GaAs is mounted on a rotating mount and heated to a temperature close to 600° C. Various sources of atoms including Ga, Al, As, and Si are placed in effusion cells with openings pointing toward the rotating substrate and controlled by shutters. The growth material is heated and the shutters control the release of the atoms into the growth chamber. The atoms that reach the substrate thermally diffuse on the surface

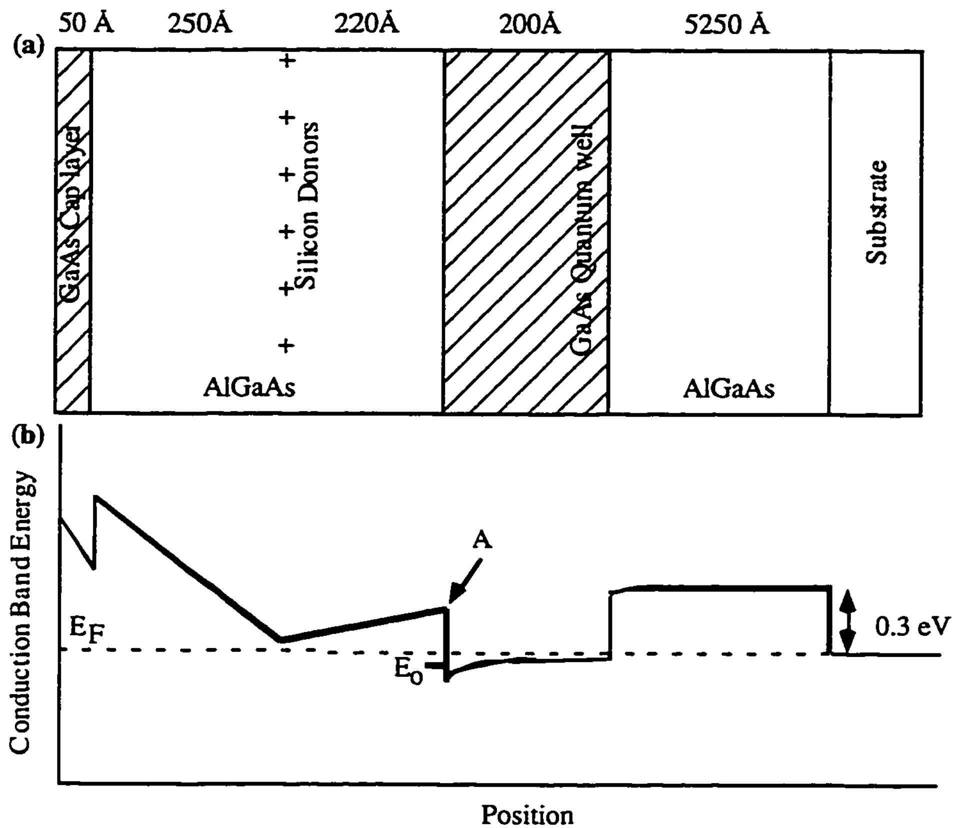


Figure 3.1 (a) Diagram showing epitaxial layer structure for wafers used to make field-effect transistors. Clear regions are $Al_{0.3}Ga_{0.7}As$, diagonal lined regions are GaAs, and the plus signs indicate silicon donors. The delta doping concentration is $\delta = 8 \times 10^{12}/cm^2$ (b) The resulting conduction band profile. The dotted line indicates the Fermi Energy and E_0 represents the energy of the first subband.

until they find a location in the crystal structure at which point it is energetically favorable for them to stick. The partial pressures of the atoms at the sample surface determine the composition of the growth material that can vary in our case from GaAs to AlAs. To provide electrons for transport in these layers the AlGaAs layer is delta doped with silicon atoms. Silicon is integrated into the crystal structure as a donor by growing it in an arsenic rich environment with the gallium shutter closed.

In this thesis we use two different heterostructure designs. Each support a two-dimensional electron gas (2DEG) while one is designed particularly for the fabrication of

freestanding mechanical structures containing 2DEGs. In these heterostructures the desired conduction band energy profile can be made by varying the aluminum concentration in $Al_xGa_{1-x}As$. Figure 3.1a shows the crystal composition for the wafer labeled 940922d, grown by Ken Campman, and used to fabricate FETs. The conduction band profile for this structure takes the form shown in Figure 3.1b. In this heterostructure electrons are thermally excited from the Si donors in the AlGaAs layer and fall into the GaAs well where they are confined to electronic subbands and limited to transport parallel to the interface. The Fermi level is pinned at the surface by a group of surface states that resides about 0.8 eV below the conduction band. The silicon donors must provide electrons to satisfy these surface states and to fill the GaAs well.

Figure 3.2 (a) shows the wafer design used to fabricate freestanding structures containing 2DEGs. This design is similar to the one shown in Figure 3.1 with the same gate side delta doping density of $8 \times 10^{12}/cm^2$ and quantum well thickness. Three additions are made to this wafer: a sacrificial AlAs layer, a substrate side 100 Å GaAs cap layer, and an additional substrate side delta doping layer. We made devices from three different wafers of this design each having a different thickness of the AlGaAs layer indicated by dimension X in figure 3.2a and a different delta-doping concentration on the substrate side of the well. The following thicknesses for X and corresponding δ-doping densities were used: X = 4010 Å and $\delta = 0$, X = 1510 Å and $\delta = 2 \times 10^{12}/cm^2$, and X = 250 Å and $\delta = 5 \times 10^{12}/cm^2$. In our fabrication process the AlAs is selectively etched away leaving the freestanding part composed of the material to the left of this sacrificial layer. As shown, the freestanding structure is capped on both sides with a GaAs layer to prevent exposure of the highly reactive AlGaAs to the air. This series of wafers made it possible to make freestanding structures with thickness of 5000 Å, 2500 Å, and 1290 Å. Figure 3.2 (b) is a schematic showing the conduction band profile. The solid line indicates the profile before the AlAs is etched away and the dotted line indicates the profile after etching that takes account of the band bending at the free surface on the substrate side of the

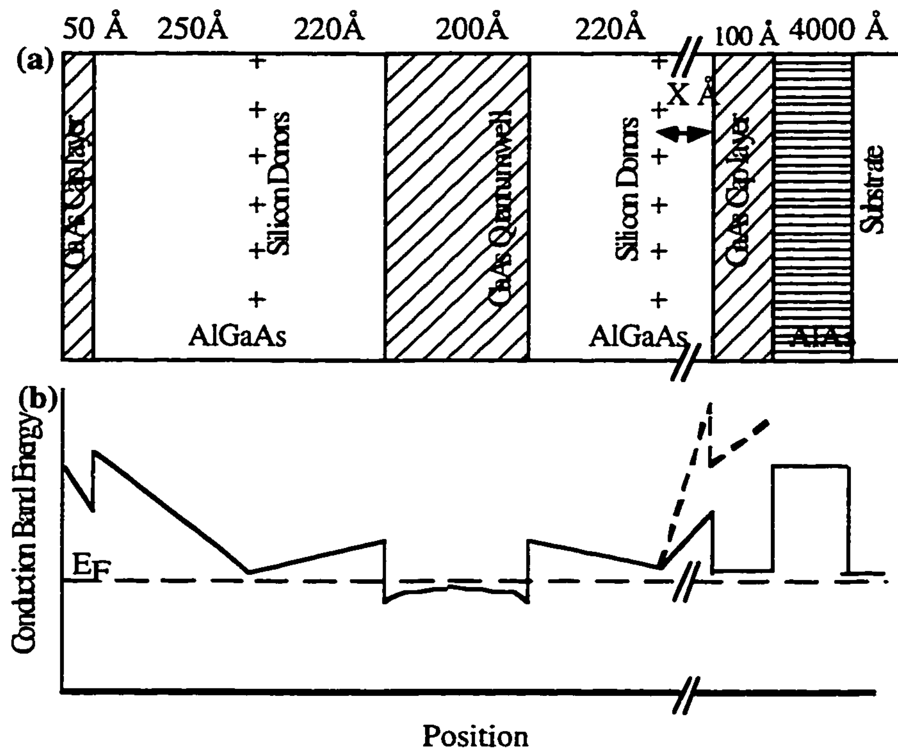


Figure 3.2 (a) Diagram showing the epitaxial layer structure for the wafer used to make cantilevers. Compositions are marked the same as in Figure 3.1. The short diagonal parallel lines indicate a break in scale. Structures of three different thicknesses were made by choosing three different values for the dimension X: 4010 Å, 1510 Å, and 250 Å. Delta-doping densities are given in the text. (b) Resulting conduction band diagram. The coarse dashed line indicates the Fermi energy. Fine dashed lines represent conduction band bending when a free surface is created on the substrate side of the quantum well after the cantilever is released.

freestanding structure.

The last two paragraphs in this section will discuss some aids in designing a wafer like the one for the freestanding structures. For this design we kept the same parameters for the well depth and thickness and the same gate side delta-doping density and position. An additional delta doping layer was placed on the substrate side of the well to satisfy the surface states that appear after the AlAs is etched away. Without these donors, the surface states will deplete the well. Group lore states that only about 1/2 of the donors are

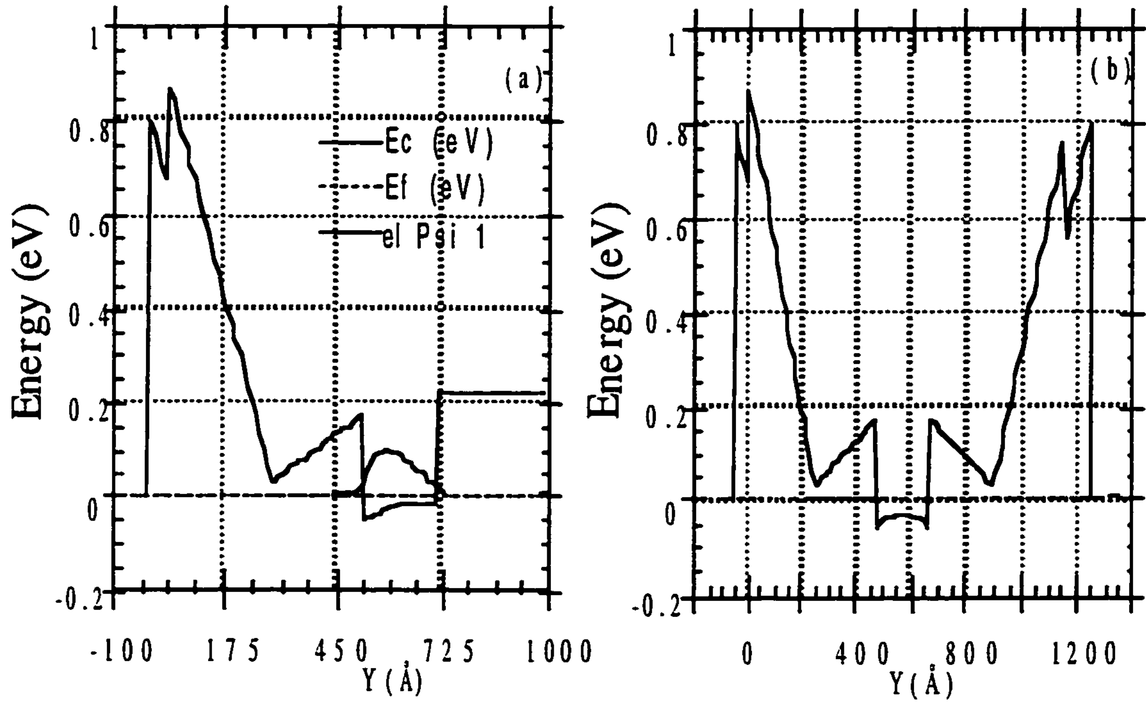


Figure 3.3 Results from the 1D Poisson/Schrodinger solver. Dark line is the conduction band, dashed line is the Fermi level and the electronic wavefunction is shown on the left. (a) Simulation of the heterostructure seen in Figure 3.1a. (b) Simulation of freestanding structure 129 nm thick with the epitaxial layers shown in Figure 3.2a.

activated and contribute electrons to the surface or to the well. We use a capacitor model to estimate the density of electrons the donors must provide to the surface $n_{surface}$.

$$n_{surface} = \frac{\varepsilon(E_{surface} + E_{offset} - E_{donors})}{be^2} \qquad (3.1)$$

where ε is the permittivity of the spacer layer between the surface and the donors, $E_{surface}$ = 0.8 V *e is the energy due to the surface potential (the Fermi energy is essentially pinned at 0.8 V below the conduction band for the GaAs surface), E_{offset} is the conduction band offset between GaAs and $Al_{0.3}Ga_{0.7}As$, E_{donors} is the depth of the silicon donor level (80meV), and b is the distance between the surface and the silicon donor level. For the 1290 Å thick freestanding structure, equation 3.1 gives a surface electron concentration of $2 \times 10^{12}/cm^2$ thus a delta doping density of $5 \times 10^{12}/cm^2$ preserves the 2DEG in the freestanding

structure.

A 1D Poisson/Schrodinger solver written by Greg Snider of Notre Dame University was useful to develop intuition concerning the wafer design. Figure 3.3 shows results from the simulation of two heterostructures, one with delta doping on only one side of the well and the other with both sides doped and a free surface on both sides of the well. While these results indicate the shape of the potential profile of the well, they do not accurately predict activation fractions of the donor level and electron gas densities. When we simulate heterostructures with an activation fraction of 1/2, the results indicate parallel conduction through the donor layer, which is not observed in the actual wafers. For the simulations shown in Figure 3.3 an activation fraction of 1/4 was used. If we allow the program to calculate the activation fraction parallel conduction is also seen. This may confirm that the simulation will not accurately predict activation fractions for temperatures less than 50 K [Snider]. For the simulation shown in Figure 3.3a, a plot of the electron wavefuction is included showing that for heterostructures with delta doping on a single side of the well the wavefunction is not symmetric about the well.

3.2 Cleaving

GaAs cleaves most readily along the {110} family of planes [Blakemore, 1987]. The preference to cleave along these planes can be understood by noticing that any atom on this plane has two out of its four bonds in the plane. Cleaving is used for three main purposes in this thesis: to cut small chips out of a big wafer for sample fabrication, to remove the unwanted substrate underneath a cantilever in order to facilitate the contact of a sample for imaging, and to prepare a chip where an underlying substrate can be easily removed from around a small cantilever by use of a deep reactive ion etch. The procedure used for cutting small chips for sample fabrication is as follows:

1. Clean a Teflon tape covered metal ruler with methanol and blow dry with N_2.

2. Place wafer on a piece of graph paper (grid size 1mm) making sure there are no particles on the surface (GaAs dust likes to stick to GaAs).

3. Carefully lay Teflon coated ruler across the desired cleave line and draw a diamond scribe lightly across the surface (the scribe's own weight is sufficient pressure).

4. Remove the sample, rinse in methanol, and blow dry (The methanol rinse decreases the chance of breathing the GaAs dust which may be carcinogenic. Wearing a dust mask during cleaving is also a good precaution.)

5. Place scribed sample on a Teflon coated glass slide with scribe mark aligned to slide edge.

6. Protect wafer on both sides of the scribe mark with filter paper and apply a small pressure to both sides of the wafer with fingers or wooden applicators. Sample should cleave along the scribe line.

7. Rinse wafer with methanol and blow dry

In order to remove the unwanted substrate beneath a cantilever to facilitate imaging, a more precise placement of the scribe mark is required. We have developed a technique involving a jig shown in figure 3.4 to draw a scribe mark on a wafer with a placement accuracy of about 10 μm. In this technique, the diamond scribe is attached to a sliding rod whose height is controlled by a small plunger below the rod that can be adjusted by means of the side lever shown in the figure. The sample is held in an aluminum groove where a plunger that can be adjusted by a 0-80 screw controls its position. A chip is cleaved in the following way. First, with no sample in the groove, the diamond scribe is drawn across the aluminum groove leaving marks of its location. The sample is then placed in the groove, and an optical microscope (magnification 100) is used to line up the desired scribe location with the marks left by the diamond. The sample is clamped, and the scribe is drawn across it. The long rod ensures that the diamond will retrace its path to within a few microns. Cleaving is accomplished by sliding the sample out to the edge of the groove

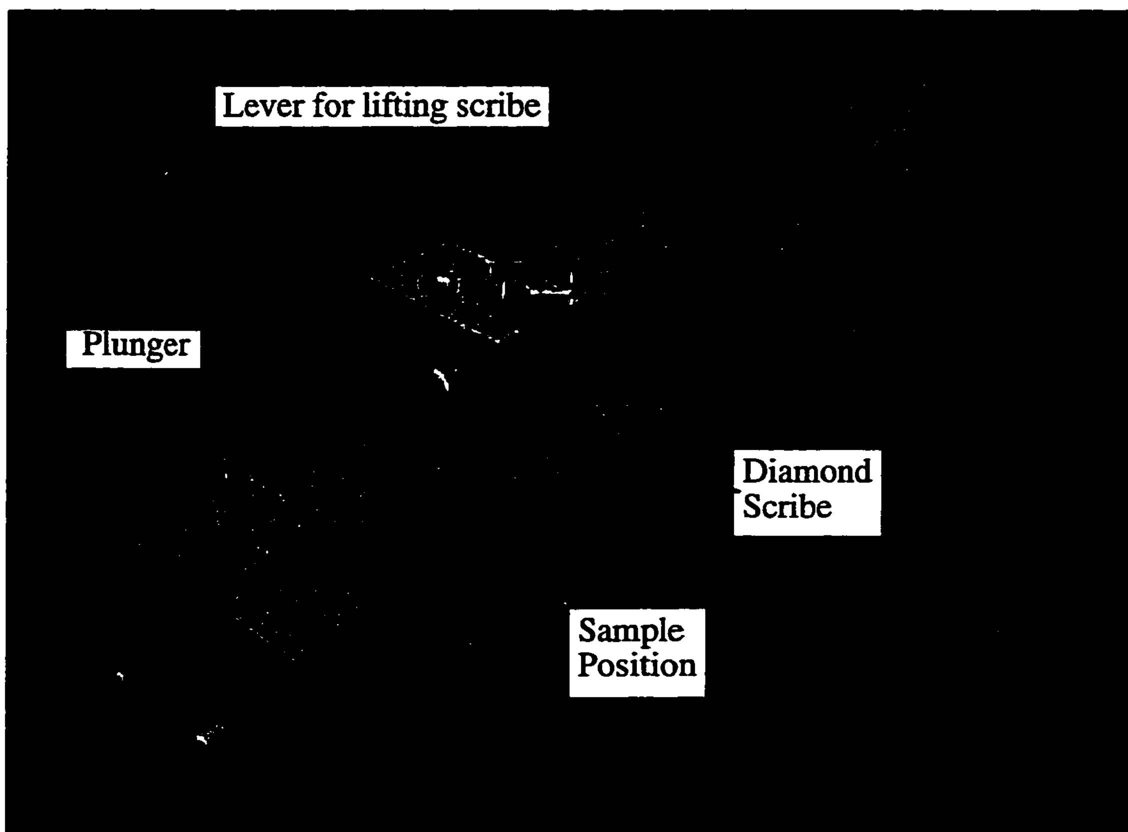


Figure 3.4 Jig for scribing and cleaving with a 10 μm placement accuracy.

where the scribe mark can be lined up with the edge of the jig, clamping, and applying a small pressure to the overhanging portion. Placement accuracy of ~10 μm has been achieved using this method.

For smaller cantilevers (with lengths ~ 3 μm) the above method cannot be used to remove the underlying substrate because the width of the scribe mark is about 2 to 4 μm making it impossible to cleave to the desired accuracy. Thus, we have developed a technique for making chips suitable for small cantilever fabrication. Most chips in the Westervelt group are cleaved along the 011 and $0\bar{1}1$ faces. This method involves cleaving along the $\bar{1}01$ and $\bar{1}10$ faces to produce chips in a boat shape shown in Figure 3.5b. As seen in the figure, this technique produces a boat shaped chip where the cleaved surfaces making up the stem of the boat form a 45° angled undercut with the sample face. The

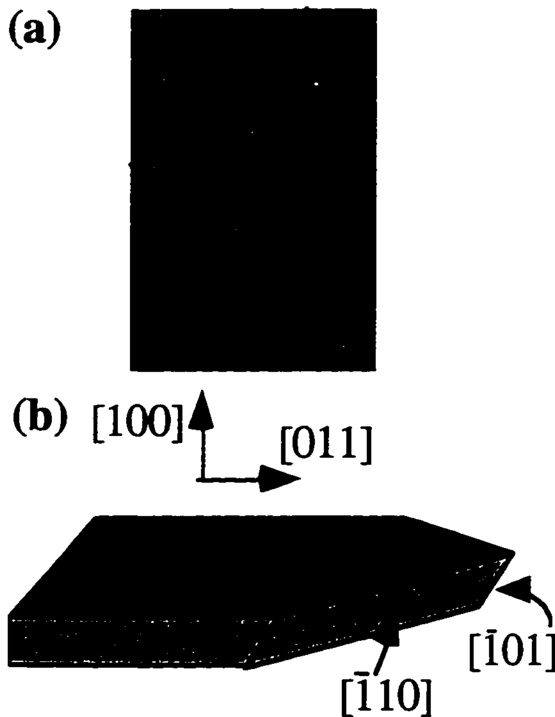


Figure 3.5 (a) Top view of chip indicating positions of scribe lines. The left, dashed line is scribed first and cleaved. A second scribe is made along the right dotted line to cleave the stern. The "point" of the boat is not touched by the diamond to improve sharpness (b) Side view indicating cleave planes.

cantilever is fabricated near the peak of the stern where the chip is relatively thin. This allows for eventual removal of the relatively thin substrate (~50 μm) near the cantilever using a reactive ion etch.

The cleaving procedure for the stern of the boat is very similar to that described above except for two main differences. The sharpest point of the stern is achieved if the diamond scribe does not touch the area that will be this peak. Thus, in step three of the above cleaving procedure the first scribe extends above and below but not through what will be the point and the second scribe approaches the point but doesn't touch it. The dotted lines in Figure 3.5 (a) illustrate the extent and position of the scribe lines. Best cleaving results were obtained by placing the scribed sample on a glass slide with no Teflon tape, lining up the scribe mark with the edge of the slide, protecting the main part of the chip with filter paper and holding it with a finger, and then pushing on the corner with a wooden applicator until it cleaves. The yield for this process is not 100% because the GaAs will occasionally cleave along the (101) instead of the $(\bar{1}01)$ plane. With some practice, this effect can be minimized.

Before proceeding to the next processing step, wafers are cleaned using a standard procedure [Katine (1996)] of 10 minutes in hot trichloroethylene (TCE), 10 minutes in acetone and ultrasound, and 10 minutes in methanol and ultrasound. The TCE cleaning step removed waxes and oils and is performed in a clean glass beaker. The sample is

placed in a small Teflon beaker with holes in it which is then placed in the TCE beaker that is on a hot plate in the fume hood. The TCE is warmed to the point where convection currents can be seen in the liquid. The acetone cleaning step removes organic contaminants and is done with the sample in a clean disposable polypropylene beaker. The methanol cleaning removes dirt and dust and is performed with the sample in a clean disposable polypropylene beaker.

3.3 Electron Beam Resist

For the subsequent electron beam lithography patterning steps we first need to cover the chips with an electron beam resist. The proper choices of resist type, layering, and thickness are crucial for the successful completion of each process step. The resist we use is polymethylmethachrylite (PMMA) dissolved in its solvent, chlorobenzene, and is applied to the chip using a spinner. We can choose between two different PMMA molecular weights or lengths, 950 K or 496 K, and three different solution concentrations, 2%, 4%, 6%. The weights are chosen based on the fact that the lower molecular weights can be exposed with lower electron dosages while a particular concentration is used to achieve the desired thickness of the layer. For processing steps involving etching, a single weight of resist is used while for thin film deposition we use a bilayer where each layer has different molecular weight. Bilayer resists are comprised of a lower 496 K PMMA layer capped by a layer of 950 K. Because the 496 K will expose at lower dosages than the 950 K, it will result in an undercut resist profile that aids in lift-off after metal deposition. For the etching steps, resist thickness is chosen based on the etch rate of the resist while for the metallization steps thickness should be at least two times the thickness of metal. The general procedure for spinning resist is outlined below

1. Clean sample in TCE using the procedure outlined in section 3.2. Move sample to inner clean room and clean with acetone in ultrasound and Methanol in ultrasound for 10

minutes each and blow dry with filtered air.

2. Rinse a glass pipette with methanol and blow dry

3. Choose the appropriate weight and concentration of PMMA and a spinner chuck with a single vacuum hole that is small enough to be completely covered by the sample. Set the spinning speed required for the proper resist thickness.

4. Place sample on the spinner, put a small drop of PMMA on the sample using the glass pipette. Immediately start the spinner and spin for 60 seconds.

5. Remove sample from spinner, place on a hot plate at T = 180° C for twenty minutes. Before baking for the full time, the quality of the resist can be observed while the sample is on the hot plate. Good quality resist will have an even coating across the regions of interest indicated by an even or slowly varying color appearing from the resist.

Repeat steps 2-5 for additional layers of resist.

For the fabrication of smaller cantilevers there was a need to perform lithography in the area 10 to 50 μm from the edge of a wafer. In this case, it is very difficult to use traditional methods for spinning resist because these methods result in a bead of PMMA ~ 10 μm thick and ~ 100 μm wide around the edge of the sample. To eliminate this on the business end of the chip, we developed and built an off-axis spinner chuck shown in figure 3.6. This chuck clamps the sample in an aluminum groove 1 inch from the spinning axis by using a small bronze spring clamp. The spinning procedure using this chuck is identical to the one outlined above except for the placement of the chip. Off-axis spinning creates a relatively even, though slightly graded, coating of PMMA near the sample edge where all the fine lithography was done.

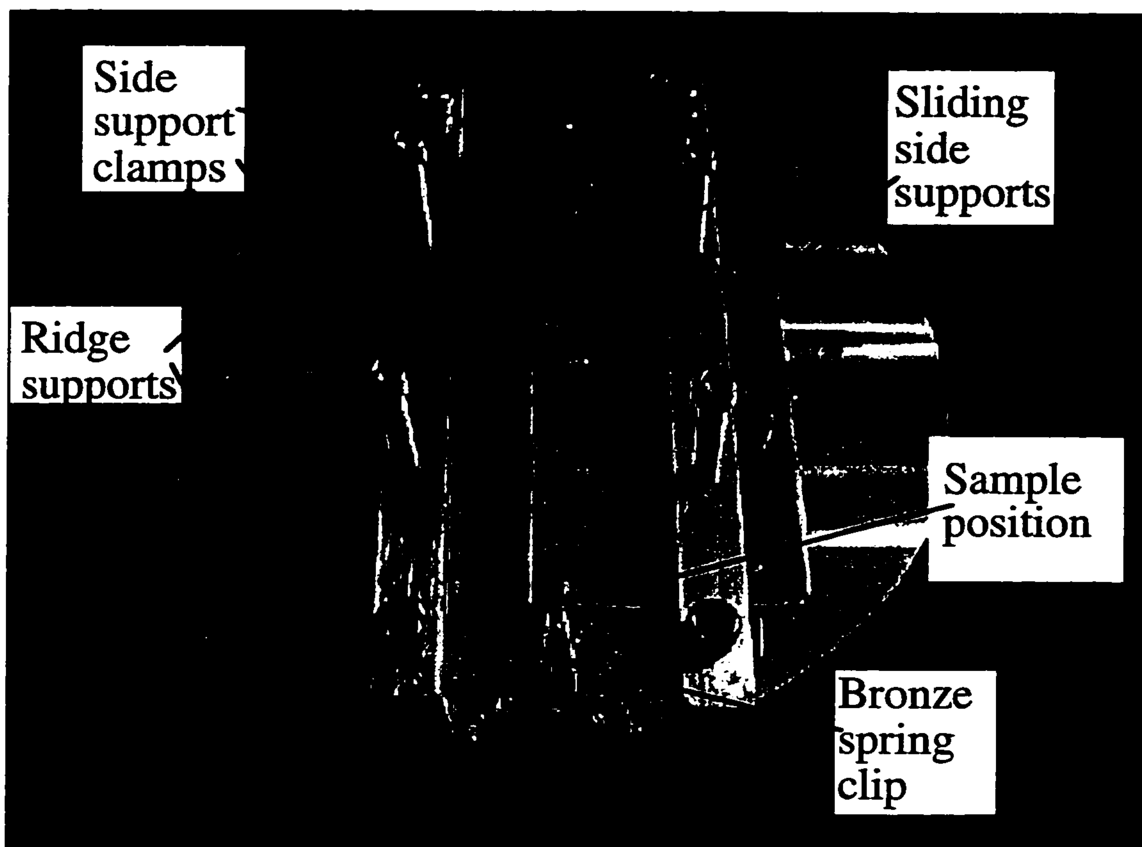


Figure 3.6 Off-axis spinner chuck. Sample is placed at the end of the spring clip against the ridge support. Chuck is attached to the spinner by a fitting on the bottom of the chuck at the center.

3.4 Electron Beam Lithography

3.4.1 Scanning Electron Microscopes

The scanning electron microscope (SEM) facility at Harvard is housed in Gordon McKay Laboratory and maintained by Yuan Lu. In general, a SEM consists of a source of electrons that are focused by magnetic lenses to a spot size limited by Coulomb repulsion of a few nanometers. Magnetic lenses control the location of the beam. For imaging, the beam is scanned across a sample while an electron detector monitors the intensity of scattered electrons. For lithography, the electron beam traces a pattern and exposes certain

areas thus changing the chemical nature of an electron beam resist. Currently there are two SEMs in Gordon McKay. The newest system is a LEO, which is a field emission microscope and is used exclusively for imaging. A field emission microscope generates electrons by thermionic emission from a sharply pointed tungsten wire. The LEO is designed for operation with higher beam current densities, closer working distances, lower accelerating voltages and can take sharp images of features down to a few nanometers. These features make it ideal for imaging low atomic number materials like developed resist structures or carbon tips and also enables it to differentiate between materials close in atomic number like chrome on a GaAs surface. For lithography we use a JOEL 6400 SEM which uses a LAB6 filament heated by a current as a source of electrons. Software written by J.C. Nabity (J.C. Nabity Lithography Systems, Bozeman, MT) directs the beam according to a DesignCAD file and enables us to pattern samples. The ease with which a DesignCAD file can be created or altered makes this lithography method excellent for design and prototyping novel structures having dimensions down to about 50 nm in GaAs. The lower feature size is limited by the backscattering of electrons from the substrate [Parikh and Kyser, (1979); Wittels, (1980)]. For silicon substrates it is possible to write features down to 20 nm but for GaAs, with higher atomic number, 30 nm is the smallest feature that has been written in our group.

Successful lithography using the JEOL 6400 is a necessary skill that needs to be mastered in order to fabricate these samples. Because transistors require three aligned lithography steps and cantilevers require five, one must be familiar with the alignment procedure. Lithography involves two main steps. The first is to prepare the pattern on the DesignCAD file and also make an appropriate run file to enable the SEM to write the pattern using the appropriate beam parameters. The second step involves SEM operation and includes aligning and writing. Below I will first outline some hints for choosing run file parameters and then give procedures for preparing the SEM, aligning, and writing samples.

3.4.2 Software

The Nabity Pattern Generation software enables us to write features with the SEM by directing the electron beam according to the pattern written in a DesignCAD file while controlling the resist exposure level based on user specified run file parameters. The DesignCAD file is written in a series of sections called layers each of which are written at different magnifications. The DesignCAD documentation and the Nabity manual are helpful in creating patterns suitable for writing. However, choosing parameters for run files requires some experience. Thus, a list of parameters and some hints of how to choose them are given below.

Origin offset: Corrects for center misalignment that occurs when writing different parts of a pattern on different magnifications or different beam currents. This can be measured by writing a test pattern consisting of different triangles written on different magnifications with vertexes sharing a common point. One can measure the shift in the resulting pattern using a calibrated optical microscope to ascertain the offset and correct for it.

Magnification: The choice of magnification is determined by the size of the pattern layer or more precisely by the farthest distance a feature is from the origin. A rough estimate of field size is 84,000 μm/magnification.

Center-to-Center (c-t-c) spacing and Line Spacing: Patterns are written by a series of spots; with the beam blanked, the magnetic actuators move its position to a certain spot, the beam is turned on, off, and moved again. This spacing is the spacing between centers of the spots. We use at mag 1000 c-t-c= 97 Å, at mag 200 c-t-c 1003 Å, at mag 20 c-t-c 6693 Å.

Measured beam current: Beam current should be measured using a small (~1 mm) hole drilled into the sample mount and in which the electron beam is focussed; the current going through the mount is measured. The PCD cup can also be used to measure the current, although its accuracy has been questioned.

Area dose: The dosage that exposes the resist. This must be determined by lithography tests.

Dwell time: Denotes the time that the beam is on at every location that it stops. This number should be above 30 μs in order to give the electronic shutter enough time to open.

3.4.3 Alignment

Both the FET and cantilever samples require multiple electron beam lithography steps that are aligned to one another to within about 100 nm. This is accomplished by first depositing markers, usually crosses whose top layer provides high electron beam contrast e.g. gold, on the sample and then using the alignment capabilities of the Nabity system to align each pattern to the same markers. Roughly, the alignment procedure involves quickly sweeping the electron beam over an area containing a marker while the Nabity software records the detector intensity. The alignment marker image is then projected onto the computer screen where electronic adjustments to the magnification, lateral position, and rotation can be made. After adjusting, a confirmation sweep is made which, if positive, is followed by writing the pattern or scanning the next alignment layer. Alignment is usually performed at three different magnifications, x 20, x 200, x 1000, each providing increased accuracy. On magnification 1000 it is very common to have alignment accuracy better than 100 nm. With the aid of the electronic adjustments, the dosage imparted to the alignment marker area is rarely enough to cross the exposure threshold for PMMA.

Alignment files are DesignCAD files that are composed of widows and overlays. Widows are made up of filled polygons of line type 1 that cover the entire area that will be scanned by the electron beam. Overlays are of line type 0 and usually outline a boundary smaller than the window and trace the alignment marker itself. In the alignment operation the window area will be scanned and the overlay will appear on the screen with the detector data. Specifications for center-to-center spacing can be calculated from suggestions in the

Nabity manual and the dwell time should be set to low values e.g. 10 μS to avoid exposing the PMMA over the alignment marker.

3.4.4 Pattern writing procedure

With all these building blocks in place I will give a procedure for electron beam lithography using the JEOL 6400 and Nabity system.

1. Mount samples on SEM mounts. The chip is placed in the desired position on the mount and a wooden applicator is used to apply some conducting carbon paint (SPI Supplies, P.O. Box 342, West Chester, PA) to both sides of the chip. Next, small flecks (~1 μm) of silver paint are applied to the edges of the chip in some non-crucial areas to provide objects to focus on. The best way to apply these small particles is to lightly rub or tap the sample surface with the splintered end of a wooden applicator covered with drying silver paint. The paint flecks should be applied to different areas of the sample in order to measure the focus at different points on the chip and ascertain its flatness. I have seen little effect on the exposure of small, 150 nm features for differences in fine focus values of up to 100 fine focus units.

2. Load sample mount into the SEM making sure that the fine working distance adjustment is set on 4 mm (This setting doesn't have to be 4 mm, but aligning is easier if the setting is the same for all steps). Move chip from center of beam location to prepare for filament saturation.

3. Load conditions from memory for operation at accelerating voltage 35 kV and working distance 39 mm.

4. Saturate the filament by turning on the accelerating voltage, making sure the detector is on and switching scan mode to line scan. Set the condenser lens (CL) to CL 12, and slowly increase the filament current until the second maximum is seen in the line scan. Operate the SEM a little below the second maximum. At this point adjust tilt to maximize

the signal then decrease CL until CL 1 is reached adjusting shift at the lower CLs to maximize the current. Return to CL 12, re-maximize tilt, go to CL 16, and press PIC, standing for picture, to change the microscope from line scan mode to picture mode and to begin imaging.

5. Measure beam currents using the hole in the sample mount and adjust fine CL to reach desired beam current of 3 pA on CL 16.

6. Orient the sample edges parallel to the raster scan axes and determine the coordinates of its corners.

7. Find a piece of silver paint and, beginning with low magnification, adjust focus and stigmate until image looks good at mag = 150,000. Adjust wobble to insure the beam is perpendicular to the sample surface. Focus on several regions of the sample and use a linear interpolation to determine the optimum focus at the device location.

8. Switch over to Nabity control and turn on external beam blanking. Roughly place the electron beam center in the device area.

9. Align

a. Begin with the lowest magnification (20 in most cases).

b. Start alignment program by typing "al 'filename'" and wait for window data to be collected.

c. Press 'b' to blank the beam and 'j' two times to show gray scale image of alignment marker.

d. Make alignment marker visible by adjusting contrast and brightness using the arrow keys with number lock off. For dimmer objects contrast limits should be closer.

e. Adjust electronic lateral position by turning Num lock on, and pressing 'Ins' until arrow keys can be used to align overlays to the alignment marker. Press 'Ins' again to adjust magnification until overlay fits the alignment marker.

f. Rotation can be adjusted (usually on magnification 200) by opening two

windows at one time with each window scanning a different alignment marker. These two windows should be in two different layers of the alignment file with the second layer tagged with a 'w' indicating that it should be written immediately after the first without a pause. Adjust window positions independently to correct for rotation.

g. After each aligning layer save the subsequent transformation matrix that includes information on lateral shifts, magnification and rotations by pressing 'enter' two times.

g. Repeat steps b through g for different magnifications and then write the pattern.

10. Run the pattern file 'pg filename a', where a activates the alignment feature, set the proper beam currents and magnifications as dictated by the program, and write the pattern by pressing the space bar. For fine features it is a good idea to write patterns with the computer screen power turned off and with little operator motion in the room, because both these actions can affect the position of the beam.

3.4.5 Developing

The exposed pattern is developed by placing the sample in isopropanol and ultrasound for 10 seconds to remove the carbon paint, developing for 90 seconds, and quenching the developer with a squeeze bottle of isopropanol. The developer consists of 375 ml isopropanol, 125 ml 4-methyl-2-pentanone (MIBK), and 6.5 ml 2-Butanone (MEK) also known as methyl ethyl ketone. For sharpest features it is a good idea to underexpose and overdevelop (use times longer than 90 seconds).

3.5 AuNiGe Ohmic Contacts

Ohmic contact to the sub-surface two-dimensional electron gas is accomplished by

thermally evaporating AuNiGe contacts followed by a thermal anneal. Annealing these contacts will thermally diffuse germanium down to the 2DEG and degenerately dope the area under the contact forming a low resistance contact even at low temperatures.

Contact evaporation is performed in the general-purpose thermal evaporator located in the clean room. This evaporator consist of a bell jar evacuated by a cryopump and containing one ground electrode and three low voltage (up to 5 V) electrodes. About 50 cm above the electrodes is an air-cooled sample mounting stage with a movable aluminum foil shutter between the sample and the electrodes. A crystal monitor is mounted beside the stage and is used to measure the depth of the deposited material.

To prepare for an evaporation, we place tungsten dimple boats (R.D. Mathis 2840 Gundry Ave. Long Beach, CA 90806), 0.01" thick, between the gold and germanium electrodes and ground and a V-shaped tungsten boat, 0.02" thick, between the nickel electrode and ground. We load the respective boats with 4 to 5 ~1 mm^3 gold chunks, a slightly smaller amount of germanium, and one nickel sphere secured with small tungsten wires that serve to improve thermal contact. The gold is cut from a Canadian maple leaf gold coin, which has a purity of 99.99%. Immediately before loading the evaporator, samples are dipped in a 1:5 solution of $NH_4OH:H_2O$ to remove native oxides and improve metal adhesion. The chips are then attached to the mount by carbon paint. Once the evaporator is loaded and the cryopump valve is open, we confirm that all the materials will melt and evaporate by testing them while protecting the sample with the shutter and then pump down to a pressure of $\sim 2 \times 10^{-7}$ Torr.

At this pressure we begin to air cool the stage and evaporate material. The general procedure for evaporating any material is as follows. After setting the crystal monitor control for the correct density, the material is cleaned by evaporating ~ 50 Å with the shutter closed. The shutter is opened to expose the samples, and the first ~30 Å of material is evaporated at a slow rate of 1 Å /sec to aid adhesion to the surface. The rate is then increased to between 3 and 8 Å/sec until the desired thickness is deposited. Using this

procedure, gold, Nickel, and Germanium are deposited in the following order and quantities:

Ni	50 Å
Au	100 Å
Ge	250 Å
Au	450 Å
Ni	100 Å
Au	400 Å

After the material is evaporated, a liftoff procedure removes the resist and leaves a metal pattern on the sample surface. In liftoff, the chip is soaked in acetone for at least four hours and then the plastic beaker containing the sample is placed in the sonicator for about 1 second. The sample is then rinsed using a squeeze bottle of acetone and is observed under acetone in a Petrie dish using an optical microscope. If liftoff is not complete, then either the soak time or sonicator time can be extended. Removing the sample from acetone and drying it before complete liftoff will make any undissolved regions of PMMA very difficult to further dissolve.

For most processes, ohmic contacts are patterned first and all subsequent patterns are aligned to the contacts. Thus, it is very efficient to include alignment marker patterns in the ohmic contact step. The topmost gold layer of the contacts provides high contrast and is thus ideal as an alignment marker. The resulting ohmic nature of the alignment marks have not introduced problems because they are electrically isolated from the FET by etch trenches.

After liftoff, annealing is accomplished using a homemade strip heater in a forming gas environment. The annealing procedure as follows:

1. Place sample on the strip heater and seal up the Plexiglas container making sure rubber o-ring is seated properly.

2. Flow forming gas (80% He and 20% H_2) with the flow-meter's silver ball on three for five minutes to completely exchange the atmosphere in the strip heater chamber. The forming gas is used to eliminate Oxygen and water vapor from the environment during

the heating process.

3. Set the thermocouple gauge on 'K' and on the Celsius scale.
4. Heat the sample to 110° C for 1 minute to remove the water from the surface.
5. Raise the temperature to 250° C for 10 seconds
6. Anneal the sample for 15 to 20 seconds at 410 to 420° C.
7. Allow the sample to cool, stop the gas flow and remove sample from chamber.
8. After annealing, observe the contact pad surface; good contacts should have the texture and appearance of baked pizza cheese.

The contact process has proven to be very robust and results in good contacts for these annealing parameters and also for higher annealing temperatures or longer annealing times. A contact is good if it behaves as a resistor rather than a diode.

3.6 Schottky Gates

The gate for an FET is produced by thermal evaporation of a layer of chrome and a layer of gold on top of a channel defined by an etch trench. The metal forms a Schottky gate which, when reversed biased, depletes the electron sheet density in the channel and actuates the FET. For low noise FETs it is a desirable for these gates to have a low metallization resistance in order to reduce the Johnson noise on the FET gate and be resistant to the formation of oxides to reduce 1/f noise. Gold has the desirable properties of a low resistivity and a resistance to the formation of oxides. However, we cannot make a contact out of pure gold due to its poor adhesion to and high diffusion rate in GaAs. Thus we use chrome, a metal which oxidizes, as a layer between the GaAs and gold. Chrome has the desirable properties of wetting the GaAs surface and preventing diffusion. Combining these two metals forms a low resistance, stable gate lead that adheres well to the GaAs surface.

The Schottky gates are deposited in the clean room using the designated Cr/Au/Al

thermal evaporator, which is very similar in form to the general-purpose evaporator described above. Ohmic contacts and Schottky gates are deposited in different evaporators to reduce the risk of nickel or germanium contaminating high resistance parts of the sample formed by the gates and thereby increasing the noise of the sample.

The main components of the Cr/Au/Al evaporator are identical to that described above. To prepare for an evaporation, we clamp a chrome rod between one electrode and ground and a tungsten dimple boat between another electrode and ground. We fill the dimple boat with 4 to 5 ~1 mm^3 gold chunks. Immediately before loading, the samples are dipped into 1:5 solution of NH_4OH: H_2O to improve metal adhesion and are mounted on the stage using carbon paint. Once the evaporator is loaded and the cryopump valve is open we turn on the current to the chrome rod to about 10% to drive off water. We then confirm that the gold will melt and evaporate and pump down to ~2×10^{-7} Torr. The desired thickness of chrome and gold are deposited following the procedure above. The total metal thickness is chosen to be about twice the thickness of any etch trench that the gate lead must cross. Liftoff follows deposition.

3.7 Etching

Etching is used for two purposes in the fabrication process: to define structures in the 2DEG by a shallow ~ 600 Å etch, and to expose underlying sacrificial layers by deeper etches up to 5000Å. We use three different methods for removing material: citric acid etching, reactive ion etching, and ion milling. These three processes span the range of available etching processes from the entirely chemical-citric acid etching to the chemical and kinetic-reactive ion etching to the entirely kinetic action of ion milling. Details of each step will be enumerated below.

3.7.1 Citric Acid/Hydrogen Peroxide Etching

In order to define FET channels in a two-dimensional electron gas system there is the need to etch through the 50 Å GaAs cap layer followed by a 470 Å AlGaAs layer containing a delta doped silicon layer to reach the well. It is not necessary to etch down to the well because the band bending due to surface states will deplete the electrons for etches terminating close to the silicon donors. However, because AlGaAs oxidizes rapidly in air it is preferable for device longevity to terminate the etch on GaAs thus creating a more stable surface. It is desirable, therefore, to find an etch which has a relatively slow, reproducible etch rate that can easily be stopped on the GaAs well and that has a low selectivity between GaAs and AlGaAs to prevent significant undercutting of the etch pattern. To this end, a citric acid/hydrogen peroxide etch procedure has been developed. Most of the details for this etching process in our lab were worked out by Berry and perfected by Mar for fabrication of low noise, low temperature FETs. I refer the interested reader to Mar's thesis [Mar, (1994)] for a summary.

This citric acid etch for gallium arsenide was first developed in the mid 1970's by Otsubo [Otsubo et al. (1976)]. Etching with a citric acid/hydrogen peroxide solution causes no observable degradation of photoresists or PMMA, has a slow, variable etch rate of 1 to 200 Å/sec which is commensurate with the shallow etches we require, and has a variable selectivity between GaAs and AlGaAs [Kitano et al. (1997)]. I would like to add that Kitano et al. have performed measurements on the selective etch rate of GaAs over AlGaAs for various pH values of the citric etch solution. They have demonstrated selectivities varying from 1 to 100 for different ratios of citric acid:Hydrogen peroxide etch solutions with pH values of 6.5. In their process the pH was adjusted by the addition of NH_4OH to the acid solution.

The citric acid solution we use is comprised of a 1:1 by weight solution of anhydrous citric acid and distilled water mixed with 30% hydrogen peroxide in a 10:1,

$C_3H_4(OH)(COOH)_3H_2O$:30% H_2O_2 solution. We heat the solution to 50° C to decrease the selectivity between GaAs and AlGaAs to about 5:1. The ratio of acid to peroxide was chosen such that the etching process is reaction rate limited as opposed to diffusion limited. In diffusion limited processes, the etch rate is limited by the rate at which the reaction ingredients are delivered to or the reaction products are taken away from the active surface by the diffusion in the liquid. This rate is very dependent on the motion of the liquid etch. To improve reproducibility, we choose a reaction rate limited process where the etch rate is limited by the chemical action of a non-etching component in the solution, which in our case is the hydrogen peroxide. This results in an increased temperature dependence of the etch but a decrease in dependence on solution agitation and thus an increased etch reproducibility for our short etch times (1 to 5 seconds). I have also noticed a variable lag time for the etch to begin. This is probably due to native oxides forming on the surface and can be eliminated by a 10 second dip in an ammonium hydroxide solution (1:5, NH_4OH(29.5% solution):H_2O) followed by a 10 second dip in an HCl solution (1:5, HCl(36-38% solution):H_20) immediately prior to etching. The etch procedure is outlined below

1. Measure PMMA thickness using profilometry.

2. Mix etch solution and place in a small glass beaker with hotplate at about 70 C and hand held thermometer measuring the etch temperature. Place a little water between the hotplate and beaker to improve thermal contact. Etch should be used when solution temperature is between 49.8° and 50.2° C

3. Dip sample in NH_4OH and HCL solutions for 10 seconds each, rinse sample with water and keep sample under water until it is dipped in the etch.

4. Dip sample in etch solution for 3 seconds, remove sample and spray water from a squeeze bottle onto sample to rinse then blow dry.

5. Measure the etch depth using the profilometer.

6. Repeat steps 3 through 5 until desired etch depth is reached.

This etch procedure works very well for large features. However, an undercut inevitably develops and can be up to five times the etch depth due to the faster etching rate of GaAs over the AlGaAs. This limits feature sizes to ~1 μm. Occasionally, the PMMA will not adhere properly to the GaAs and will allow for much larger undercuts that form in random places. This problem may be eliminated by using a primer to prepare the sample surface before spinning resist to achieve a more uniform adhesion. We have not used such a primer and I'm not aware of the existence of one. Further development is needed for reliable and reproducible ~1 μm etches using citric acid.

3.7.2 Reactive Ion Etching

Reactive ion etching (RIE) is a dry etch process involving relatively fast etch rates that can be used for the fabrication of structures with high aspect ratios. A typical reactive ion etcher consists of a chamber connected to a vacuum system containing two electrodes between which a gas at pressures varying from 0.1 mT to about 200 mT can be introduced. A sample is placed on the lower electrode that is capacitively coupled to a radio frequency generator (most commonly set to 13.56 MHz) with a matching capacitance network that can be tuned to reduce the power reflected to the generator. The etching gas is introduced, and an RF signal is applied to the sample electrode. The gas is ionized by the RF thus producing a plasma containing electrons, ions and free radicals. Because the net current on the lower plate must be zero and the mass of the ions and electrons are vastly different, a negative dc bias is produced on the lower plate. This serves to accelerate the ions toward the sample where they impart their energy to aid in the chemical etching process and also sputter material away. The highly reactive, neutral free radicals diffuse towards the sample where they adsorb onto the surface. On the surface, they chemically react with the sample with the aid of the energy imparted by the ions and form volatile products that are

evacuated from the chamber by the pump. The ion assisted reaction makes possible anisotropic etches that produce high aspect ratio structures.

The etching of GaAs can be done with many different gases of which the most common include CCl_2F_2 [Knoedler et al. (1986)], CCL_4 [Klinger et al. (1982)], Cl_2/Ar [Lee et al. (1996)], C_2H_6/H_2 [Pearton et al. (1989)], BCl_3[Wu et al. (1995)], and $SiCl_4$ [Pearton et al. (1990)]. Because we need to etch away epilayers containing GaAs and AlGaAs, we need an etch gas that will work on the tough oxides that form on the aluminum containing compounds. To this end we have used two different etching gas combinations: chlorine/boron trichloride [Tamura et al. (1984)] and silicon tetrachloride/boron trichloride [Pearton et al. (1990)]. Both etches exhibit little lag time (time between plasma ignition and the initiation of etching) and easily etch through aluminum containing compounds including AlAs.

A brief overview of the etching chemistry of the Cl_2/BCl_3 system may be helpful if the reader would ever intend a further application or adaptation of the etching process. Although I have not been able to find any literature that unequivocally claimed a detailed knowledge of the etching process and subsequent reaction products, I will list below some of the empirical observations as well as the tentative conclusions concerning the chemistry that can be drawn from them. It is believed that etching is performed by free chlorine radicals produced in the plasma that adsorb onto the surface and form volatile $AsCl_3$, $GaCl_3$ and AlCl, $AlCl_2$ or $AlCl_3$ [Pearton et al. (1990)]. However, before etching, it is necessary to first break through native oxide layers, and during etching it is necessary to insure that no inert molecule or atom impedes further reaction. The following observations have been made concerning chlorine etching. It is observed that a Cl_2 system will etch GaAs but not its oxide, nor will it etch AlGaAs [Smolinksy et al. (1981)]. If a non-reactive sputtering agent, like Ar or He_2, is added to the Cl_2 then both AlGaAs and the Gallium oxide can be etched [Pearton et al. (1990)]. However, etching only occurs in chambers that have very low levels of residual oxygen or water vapor (acceptable levels can be achieved in RIE

chambers with load lock sample insertion bays [Tamura et al. (1984)]). If there is a large residual oxygen or water level in the chamber, which is the case with our system that has stainless steel walls exposed to air most of the time, then a Cl_2 plasma yields an imperceptible etch rate even for GaAs. Thus, it is necessary to introduce boron trichloride as an oxygen and water vapor scavenger. Because the relative reactivity of BCl_x is higher than that of Al for the production of oxygen compounds, BCl_3 will scavenge the residual oxygen in the etching chamber and prevent a robust oxide from forming on the AlGaAs and impeding the etch [Tokunaga et al. (1981)]. The addition of BCl_3 mixed with Cl_2 has resulted in etches with no lag time giving evidence that it is a good etcher of GaAs native oxides and that it is a good scavenger of oxygen and water vapor. Increasing the Cl_2 concentration relative to BCl_3 increases the etch rate. This enhancement is probably due to two processes (1) the Cl_2 reacting with BCl_3 to form two active etchants BCl_2^+ ions and $\dot{Cl}$ free radicals and (2) Cl_2 reacting with adsorbed, inert boron to form volatile BCl_3 thus exposing the surface for further etching. The ratio of $Cl_2/BCl_3 = 0.2$ was found to give the most reproducible, anisotropic etch rates with smooth bottomed etch profiles [Tamura et al. (1984)].

Two different etching machines have performed reactive ion etching for our processes. The $SiCl_4/BCl_3$ gases are used in a reactive ion etcher located at the Micro-Fabrication Lab at MIT in building 13 and the Cl_2/BCl_3 gas combination is used in the RIE in the Gordon McKay clean room. Because the future of the MIT Microlab is uncertain, as is use by us as outside users, I will limit my description to the Harvard machine. The Harvard RIE was purchased from the now defunct Plasma Science Incorporated. The chamber houses two 8" diameter stainless steel electrodes and is pumped by a Varian 70 turbo pump which is backed by an Alcatel CP-300 mechanical vacuum pump that has a pumping speed of 11 cubic feet min^{-1}. Gas flow is regulated by MDC mass flow controllers and delivered to the chamber via a perforated gas delivery ring between the 8-inch electrodes. The adjustment of this gas flow combined with the position of a butterfly

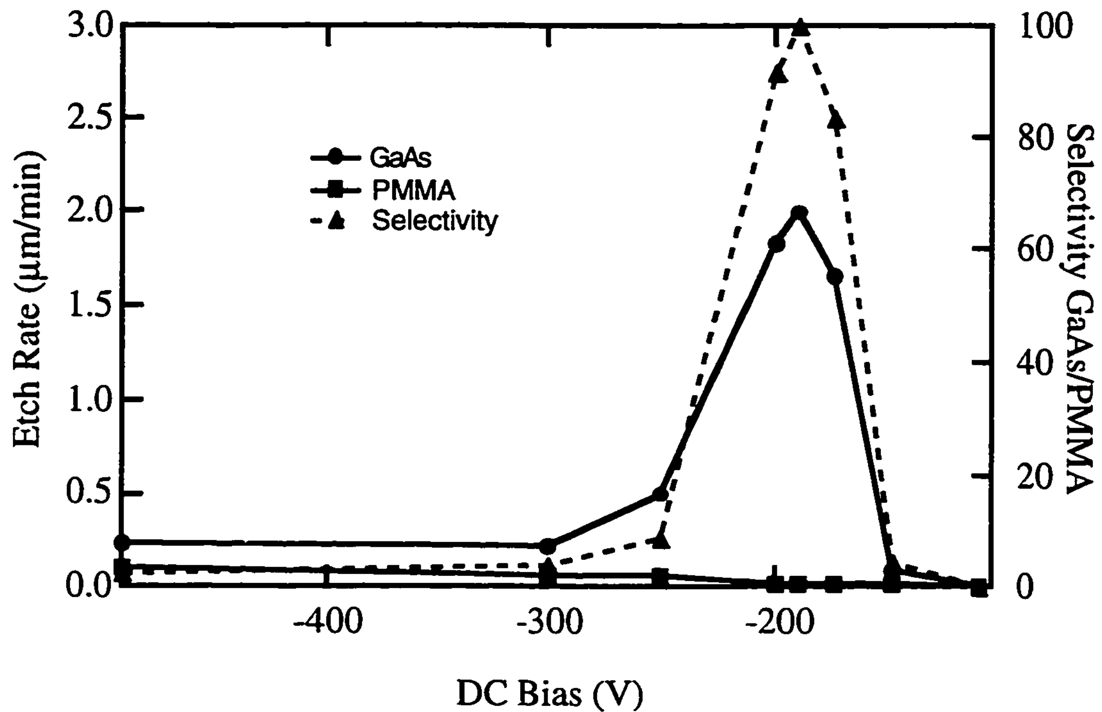


Figure 3.7 Etch rate as a function of DC bias for a flow rate of 3.9 sccm of BCl_3 and 2.6 SCCM of Cl_2, the butterfly valve was closed during etching. Power was adjusted to maintain DC bias throughout the etch. Typical PMMA etch rates varied from 0.02 µ/min at –200 V to 0.06 µ/min at –500 V. Maximum selectivity was obtained at –200 volts.

valve between the turbo and chamber controls the gas pressure in the chamber. Chlorine etch pressures can vary between 0.5 mT and 60 mT. The RF generator was built by Plasma Science and is connected to a capacitance-tuning network that is manually tuned by an adjustment knob on the front panel. The RF power or dc bias can be set and tuned for each etch.

Figure 3.7 summarizes the characterization that we have done on the RIE using GaAs as a test. These samples were etched with a BCl_3 flow rate of 3.9 standard cubic centimeters per minute (sccm), Cl_2 flow rate of 2.6 sccm, the back valve of the RIE closed, and a power that was adjusted to keep the DC bias constant during the etch. Before etching, the samples were dipped in $NH_4OH:H_2O$, 1:5 to remove some of the native oxides. We also found an extensive dependence of etch rate on the cleanliness of the

Figure 3.8 SEM image of a 3 μm x 2 μm cantilever, indicated by the arrow in the image, fabricated near the point of a chip. The substrate ~7 μm away from the cantilever tip has been removed with a BCl_3/Cl_2 RIE.

chamber; if the chamber was scrubbed with Scotchbrite and isopropanol and wiped dry with a cleanroom wipe before each use the system would exhibit a fairly predictable etch rate. With dirty walls, the plasma may in fact deposit material etched from the walls onto the sample! Each data point is taken using a freshly cleaned, unetched sample. We found that once a sample was etched a barrier formed on it preventing etching from beginning again. This is a particularly troubling characteristic because it is difficult to etch to the desired depth the first time. This makes it very hard to perform controlled etches short of a constant characterization of the machine and process.

The maximum etch rate occurred at a DC bias of 200 V. We don't understand why

a peak in etch rate occurs for this setting. One possible explanation is that for higher dc biases more material is being etched off the walls and is deposited on the sample. Etch rate for PMMA is relatively constant for increasing DC bias and is generally small; at 200 volts the etch rate is 0.02 μm/min and at 500 it increases to 0.06 μm/min. This behavior may indicate that the PMMA is mainly being etched by the kinetic motion of the ions rather than any chemical assisted process. Selectivities of up to 1:100 for resist etch rate: sample etch rate make possible very deep etches ~ 100 μm using easily obtained resist thickness. Figure 3.8 is a SEM image of a 3 μm cantilever where the RIE was used to etch the nearby substrate. The etch rate was approximately 1 μm/minute and was very isotropic as can be seen from the curved sidewalls.

Using an RIE with boron trichloride demands some special features of the system and some special operating procedures. Boron trichloride, when mixed with water vapor, will form hydrochloric acid that erodes pumps, valves or gas lines. To prevent HCl condensation on the bearings in the turbo pump, a valve is installed in the motor chamber through which 25 sccm of nitrogen gas flows to keep these parts constantly overpressured. Special care must also be taken when using a backing pump that uses oil. First, the pump should be charged with Fomblin oil, which is rated for its low absorption of O and the pumping of caustic gases. However, even with this special precaution, it should be noted that hydrochloric acid is miscible with Fomblin oil. The resulting HCl oil solution corrodes the pump and covers the innards with a guacamole-like substance that will etch through a piece of aluminum foil in less than a day. In order to maintain a working system the oil must be filtered using an external oil filtration system containing activated alumina filters to cleanse the oil from dissolved HCl. When venting the chamber after using BCl_3, care should be taken to insure that the lowest pressure of the system is at the chamber. This ensures that no BCl_3 will diffuse into the turbo pump or gas lines. This can be accomplished by venting the system from the bearing purge ports on the turbo instead of using the gas distribution ring.

The RIE promises to be a valuable tool for removing large amounts of material quickly and with a relatively thin etch mask. However, because of the isotropic nature of this setting, it is not useful for etching small features. More anisotropic etch rates have been achieved using different parameters that have much slower etch rates and much lower resist selectivities.

One major disadvantage of using the RIE is the danger involved with these gases. Boron trichloride will form HCl vapor in air and Chlorine is one of the most dangerous gases used in the lab; air with 7 ppm Cl_2 can cause respiratory irritation and several breaths at 20 to 30 ppm can cause death.

3.7.3 Ion Milling

Ion milling relies on the kinetic motion of ions to bombard the surface of a sample and physically sputter material away. We have found this process useful to define FET channels in the 2DEG and for deeper etches to expose an underlying sacrificial etch layer. The kinetic nature of this process and the lack of any reliance on chemistry means ion milling processes produce very robust and reproducible etch rates even through the reactive epilayers of different compositions found in our samples. For example, unlike the RIE, ion milling can be interrupted, the sample exposed to air and measured, and then loaded back into the ion miller to continue sputtering. The violent nature of this etch process is its main disadvantage. The ion impact doesn't only remove material but also damages the underlying, unetched layer. Swaminathan et al. studied the photoluminescence of a quantum well 40 nm from a milled surface and found significant damage for ion energies greater than 500 eV [Swaminathan et al. (1991)]. Ion milling is a plausible option for us only because our applications are not sensitive to this damage. We have also found little evidence of lateral damage or degradation in our ion milling of narrow channels of order 1 μm. Finally, we have found milling produces smooth surfaces that adhere well to Cr/Au

films that are deposited on them and even allow wire bonding to these films. For all these reasons we have found ion milling to be a robust, reliable way to remove material to form the FET channel and for defining cantilever structures.

An excellent description of the ion miller in the Gordon McKay cleanroom as well as a detailed operating procedure can be found in the thesis by Niraj Anand, a former student of professor Tinkham [Anand, (1995)]. Another former Tinkham student, Gabriel Spalding, built this ion miller. Its main components consist of a central vacuum chamber that is evacuated by a cryopump, an ion gun that creates a plasma of Ar and accelerates Ar ions toward a sample and a rotating target for the sample mount. At the target, the beam covers an area about 4" in diameter with a measured uniformity of about 10% over a 1" area. We have marked the position of the target for 90° incidence of the ion beam and found that the center of the beam (corresponding to the largest etch rate) is about 0.5 inches from the left side of the target and 1.5" down from top row of tapped holes. The target and gun are both water cooled during milling.

Typical etch rates for GaAs/AlGaAs heterostructures are 1 nm/sec for a beam voltage of 500 V and current of 23 mA and an accelerating voltage of 300 V, discharge voltage of 40 V and the ions incident 90° to the sample surface. This etch rate has been found to be linearly proportional to the current density of the beam [Chen et al. (1986)]. Little dependence of etch rate on material composition has been observed. Resist etch rates for PMMA are 0.6 nm /sec. It should be noted that the high-energy ions not only etch PMMA but also cross-link it. The PMMA therefore should be made especially thick in order to ensure the existence of a non-cross-linked layer of PMMA next to the sample that can easily be dissolved in acetone. We have successfully removed resist with a thickness of 1 μm after 4 minutes of ion milling.

Ion milling is reliable but has its limitations on milling depth due to the relatively low selectivity 1.6 of GaAs to resist. The need to leave an uncrosslinked region further limits the depth. It is possible to strengthen resists using a metal layer. This may be a

slightly better option but metallization of the resist will not allow much deeper features to be etched due to 1:1 mill rates of GaAs to most metals. Thus for our deepest features of 0.5 μm this method has proved reliable but for deeper features with high aspect ratios the RIE, with its fragile processes, is still the preferable etching technique.

3.8 Hydrofluoric Acid Etching

Once the cantilever has been laterally outlined using electron beam lithography and the surrounding, underlying layer of aluminum arsenide has been exposed by an etching technique, then the cantilever is ready to be undercut and freed from the substrate. This is accomplished by using hydrofluoric acid with its extremely high selectivity for etching aluminum arsenide over gallium arsenide. Selectivities have been measured to be $\sim 10^9$

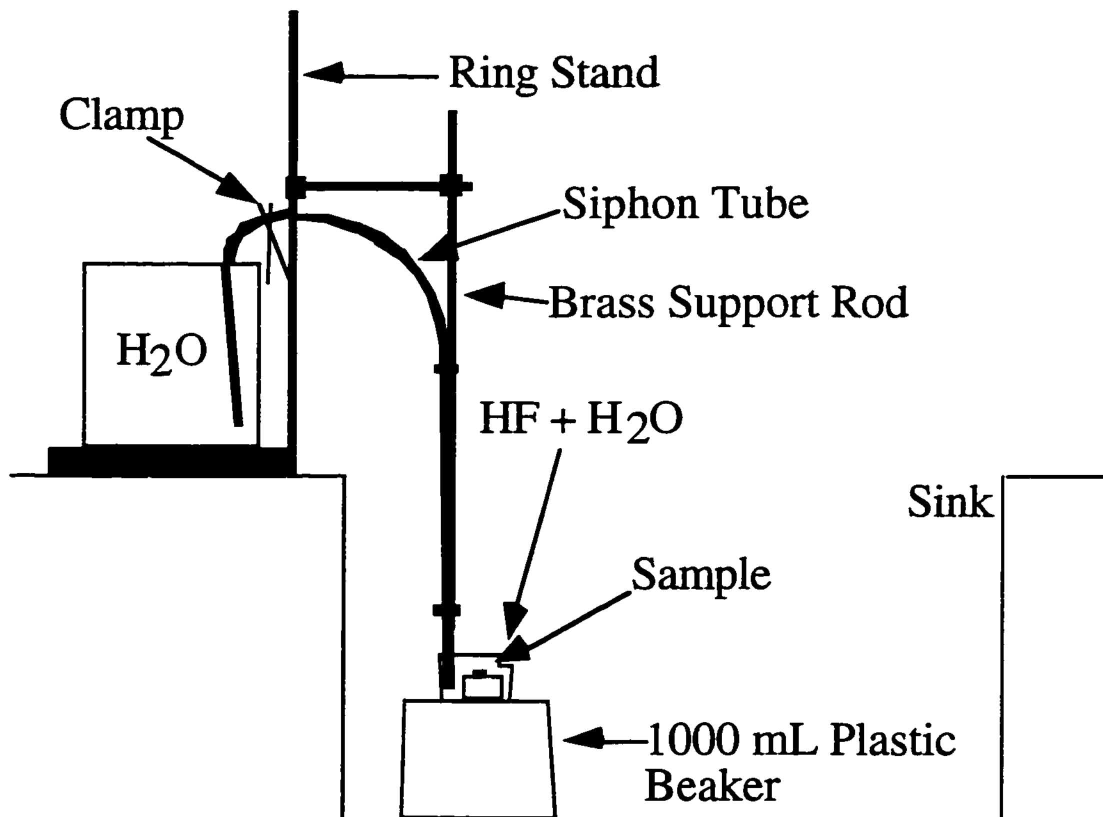


Figure 3.9 Schematic of experimental setup for hydrofluoric acid etching.

[Yablonovitch et al. (1987); Wu, X. S. et al. (1985)].

Because of the fragility of a large suspended structure, it is important that the sample not be taken through a liquid air interface after it is freed from the substrate. This makes quenching the acid etch not as simple as pulling the chip out of HF and dipping it in water. To this end we have developed a dynamic flushing system that exchanges the acid with distilled water while limiting the turbulence experienced by the fragile mechanical structures.

Figure 3.8 shows the experimental setup for the HF etch. Etching is carried out in a sink with the tap water running throughout the time of the process. The sample sits on top of a Teflon block in a polypropylene beaker that rests on an upside-down, 1000 ml polypropylene beaker. The acid solution is placed in the sample beaker and is eventually quenched by siphoning distilled water from a raised 1000 ml beaker through a Tygon tube. The siphon is supported by a ring stand and brass rod and is opened or closed by vise grip pliers. A gentle exchange of the acid is achieved by taking care to lower the siphon end below the top of the Teflon blocks so the turbulence will not move the chip and also by including a notch in the beaker to provide a preferential direction for liquid to exit.

A typical etch procedure is as follows. First, the Teflon blocks along with 15 ml of distilled water are placed in the sample beaker that is sitting on the stand. The Tygon siphon is charged, clamped with the vise grip pliers, and lowered into the sample beaker. Care should be taken at this step to ensure that there are no air bubbles in the siphon and that its end extends below the Teflon blocks. Once the apparatus is set up, hydrofluoric acid is added to the sample beaker. A 1:15, HF(49%):H_2O solution will laterally etch AlAs at a rate of 0.6 μm/sec while 1:5 solution etches at about 1 μm/ sec. Higher concentrations of HF violently attack AlAs and may destroy the top epilayer in the etching process. The sample is then dipped for 10 seconds each in the NH_4OH and HCl solutions (with the same concentrations as described in section 3.7.1) to remove native oxides. This process is then quenched by dipping the sample in distilled water. The sample is then immediately placed

in the HF solution. At the appropriate time, the siphon is unclamped and approximately 800 ml of distilled water are allowed to flow through the sample beaker to completely exchange the HF solution. The exchange takes approximately 15 seconds. The success of the etch can be determined by viewing the sample in liquid under an optical microscope. The sample is taken off the Teflon blocks and placed on the beaker bottom, the blocks are removed from the beaker and the water level is lowered using a pipette. Under the microscope, the lateral extent of the etch can easily be seen as a colored "halo" around the regions that had AlAs exposed. If more etching is required the HF procedure can be repeated keeping the sample under the liquid at all times. The sample can be kept under liquid by setting up the sample beaker and siphon while the sample is still in the beaker. The HF is then added to the sample/water in the beaker and the etch is quenched at the appropriate time. A reduction in HF concentration may be helpful in controlling the extent of the second HF etch.

For the next processing step, the distilled water must be exchanged by ethanol. This can be accomplished using a siphon, in a similar way described above. However, it is difficult to charge the siphon because a clamped Tygon tube will not support ethanol under the force of gravity. Because timing is not crucial for this exchange, we chose the simple method of using a funnel instead of a siphon. We place the sample on the Teflon blocks under water and then put the end of a long stemmed funnel in the position that the siphon held and simply pour 800 ml of ethanol through the funnel to exchange the water. The sample is now ready for the next step.

3.9 Passivation

Immediately after the first on-cantilever FET emerged from the critical point dryer, I measured the channel resistance and then went to the annual group dinner intending to come back and mount the device in a Dewar for measurements. Upon my return, I

rechecked the channel resistance and found it to be infinite. I thought I had destroyed my device. After a careful observation with the SEM, I saw no damage and this led me to consider the prospect of the sample oxidizing and the need for passivation.

It is well known and documented that it is necessary to passivate GaAs devices to preserve their electronic or optical properties over time. A common technique for passivating GaAs ICs is to use a silicon nitride layer [Asbeck et al. (1984)]. For optical applications, groups have experimented with passivation using hydrogen ions [Chang, Ying-Lan, (1995)], selenium [Sandruff et al, (1989a)], arsenic sulfide [Sandroff et al. (1989b)], and sulfur pentasulfide [Lee, H.H. et al. (1989)]. For our structures, not only do we have an exposed GaAs surface but also much more reactive AlGaAs surfaces and a highly reactive AlAs surface. Because we desire to fabricate cantilevers with thicknesses ~130 nm it is difficult to grow thin, continuous passivating layers, like silicon nitride, that would not seriously affect cantilever mechanical properties. Thus we limited ourselves to the search for monolayer or single molecule passivation layers that would not affect the mechanical properties of the device.

In response to my explanation of this passivation problem Joe Tien, a graduate student of Professor George Whitesides, who was working with self-assembled monolayers (SAMS) pointed out a 1992 article by Colin Bain [Bain, (1992)] who explained Allara's development [Sheen, (1992)] of self assembled monolayers of long chain thiols on clean GaAs. The Whitesides group had a bottle containing a C-11 fluorinated thiol solution that allowed us to easily perform a test of its passivation ability. The molecule $HS(CH_2)_2(CF_2)_{10}CF_3$, consists of a sulfur atom bonded to a hydrogen atom and attached to one of a pair of two CH_2 units. The other CH_2 of the pair is attached to the end of a chain of 10 CF_2 units capped with a CF_3. We soak our samples in a solution of 5 mM $HS(CH_2)_2(CF_2)_{10}CF_3$ in ethanol to form a monolayer on our samples. The molecules form a monolayer by the sulfur bonding to every other arsenic atom such that the molecule makes an angle 57° with the normal. We have found that ordered monolayers will form a

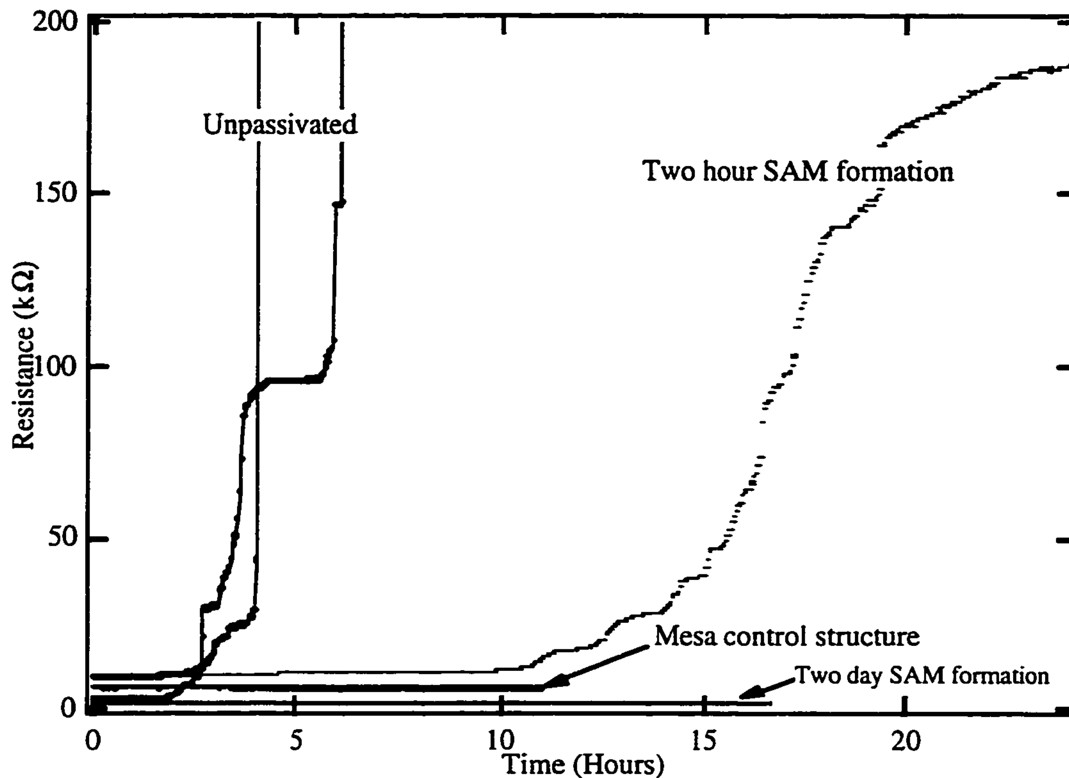


Figure 3.10 Graph of resistance verses time for passivation test samples. Traces are shown for unpassivated samples, samples with a SAM formed in a two hour period, and two day period. Data labeled mesa control structure are from a sample taken through the same process steps, NH_4OH, HCl, and HF, but with no undercut. The resistance of the mesa and two-day SAM were constant for at least one month.

very good barrier to oxidation for periods approaching months.

To measure the effectiveness of the passivation layer, we fabricated test structures consisting of two ohmic contacts separated by an etch trench and linked by a suspended bridge across the trench. The bridge was fabricated by electron beam lithography, a citric acid etch to expose the underlying layer of AlAs, and a hydrofluoric acid step to release the bridge from the substrate. A passivation procedure was then performed on the bridge and the sample was brought into the air by a critical point dryer. Wirebonds were attached to the sample and its resistance monitored every five minutes for however long the current path was continuous.

Figure 3.10 shows the resistance as a function of time for bridges subjected to

different surface preparation procedures. While the resistance of unpassivated samples would increase and become immeasurable after about 3 hours, samples coated with monolayers showed much better performance. A self assembled monolayer will form in a few seconds on the GaAs surface, a fact verified by observing the transformation from a hydrophilic, clean GaAs surface to a hydrophobic, SAM covered surface after a few second dip in the SAM solution. However, as the data in figure 3.10 show, a monolayer formed over a period of two hours will easily break down and allow air to penetrate the sample in ~ 1 day. SAM formation is an equilibrium process; as the sample sits in ethanol, molecules will continuously adhere to the sample while others dissolve into the solvent. This dynamic process will perfect the structure of the monolayer and result in a barrier that is significantly less permeable to air. The technique resulting in the longest device lifetime involved a SAM that was allowed to form over a two-day period at room temperature. A graph of resistance verses time for the sample with a two-day SAM is shown in Figure 3.9. The resistance for this device was measured to be constant for about 1 month. It is interesting to note that when the dip is the NH_4OH and HCl solutions is missed then the sample resistance becomes immeasurable in about three hours. In this case a two day soak in the SAM solution leaves the sample behaving as if it was unpassivated.

The procedure for depositing a self-assembled monolayer (SAM) on GaAs will be given below. First, prepare a solution of C-11 SAM dissolved in ethanol in a ?? concentration. Dip the samples in the NH_4OH and HCl solutions (for 10 seconds each) to remove native oxide layers that will seriously impede SAM formation; this should be done before the HF step. After freeing the mechanical structure in HF and replacing its ambient liquid with ethanol, transfer the sample into a plastic beaker containing the SAM solution using a very shallow Teflon beaker that keeps the sample under ethanol but doesn't transfer much liquid to the SAM solution. Cap the plastic beaker with aluminum foil to minimize evaporation during the two day, room temperature SAM formation process.

3.10 Critical Point drying

Once a mechanical structure is freed from its underlying substrate using hydrofluoric acid, it must be removed from liquid into air. If the structure is small, this can be accomplished by simply removing the sample from the ethanol beaker with a pair of Teflon tweezers, placing it on a piece of filter paper, and allowing it to dry in air. I have had success using this procedure for cantilevers with lateral dimensions of 3 μm x 2 μm. However, as the area of the suspended structure becomes larger, surface tension effects grow and complicate the removal process. When the sample is being removed to air, some liquid remains between the suspended structure and the substrate. This liquid can reduce its surface energy by drawing the suspended structure towards the substrate until it makes contact. Once the liquid dries, it deposits any non-volatile residual particles that were suspended in it and these serve to cement the structure to the substrate. Van der Waals forces also add to the forces of attraction and adhesion although they have been found to be smaller than the cementing action of the residual particles. This effect, termed "sticture" in the literature, serves to permanently adhere the suspended structure to the substrate [Alley, (1992)].

Many different methods have been developed to eliminate or reduce this problem. One class of solutions involve reducing the adhesion between the two surfaces by chemical treatment after etching and before drying [Deng, (1995)]. Other methods seek to reduce surface tension either through an appropriate choice of liquid (e.g. methanol) or by heating the liquid before sample removal [Abe, (1995)]. Still other methods seek to remove surface tension all together either by freezing the liquid and allowing it to sublimate or by bringing the liquid into a region in its phase diagram where there is no boundary and hence no first order phase transition between liquid and gas. The latter method is called critical point drying.

Our samples present some constraints to our choice of drying methods. First, in

order to preserve the passivation monolayer we do not have liberty to significantly alter the surface chemistry. Second, because sample drying is the final step of an approximately three week process, we do not want to face the risks associated with a mere reduction of surface tension nor the potential dangers of the freezing process. Thus, we choose critical point drying using carbon dioxide, the method with the highest yield, as the best way to dry our samples. I have dried approximately 40 samples using this method and have not lost one due to a failure of the drying process.

The process of critical point drying can be understood by looking at a phase diagram [Bartlett, (1975)]. Figure 3.11 shows a phase diagram for CO_2 and indicates an acceptable path taken for a drying process. First, the temperature is reduced below room temperature and liquid CO_2 is allowed into a chamber (point A). The chamber is sealed and heated. As the temperature approaches the critical temperature T_c the liquid's heat of vaporization approaches zero and at T_c it passes into the gas phase with no effects of surface tension. Temperature is raised further to reach point (B). Pressure is then reduced to atmospheric pressure while maintaining the higher temperature (between 35-40° C) to go around the critical point to reach point C. Once cooled, the sample has been safely brought to the air at room temperature and pressure (D). Care should be taken to ensure that the chamber is not less than half full of liquid

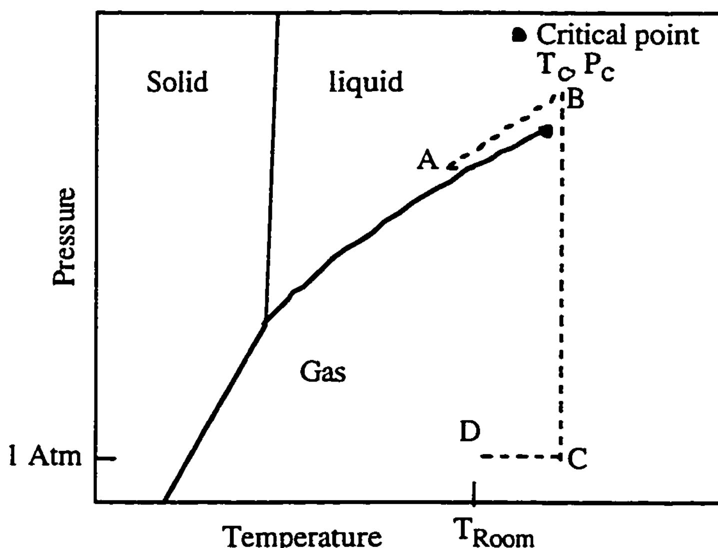


Figure 3.11 Schematic of the phase diagram for CO_2. Dotted line indicates path taken in the critical point drying process.

before heating begins; in this case the liquid will simply boil into the gas phase and the sample may be destroyed.

The critical point dryer consists of a stainless steel chamber, three needle valves and two switches, one for light and one for heat. The drying chamber, designed to withstand high pressures, is a hollow cylinder of stainless steel with a glass bottom which allows light into it. This chamber is capped with a removable flange containing a glass observation window. An unregulated CO_2 cylinder is connected to the dryer and controlled through a needle valve while another needle valve controls an exhaust port. Chamber temperature can be reduced by means of a third valve that reduces the temperature by allowing pressurized CO_2 from the cylinder to expand outside the chamber and remove heat. An electric heating coil accomplishes heating.

The procedure for critical point drying is as follows. We begin with the sample in a beaker of ethanol. We lower a wire mesh basket into the beaker, place the sample in the basket and cover the basket using a tight fitting mesh lid. The basket can be removed from the ethanol beaker without exposing the sample to air because surface tension prevents the ethanol from draining out of the basket. Next, the drying chamber is partially filled with ethanol and cooled to about 0° C. The wire mesh basket containing the sample is then placed in the chamber and secured by placing empty wire mesh baskets around it. The chamber is sealed and cooled to about 0° C. Liquid CO_2 is allowed to flow into the chamber at a pressure of about 800 PSI and mixes with the ethanol. After the chamber is full of CO_2 and ethanol, the exhaust valve is opened to dynamically flush the chamber with liquid CO_2 until the ethanol is removed and completely exchanged by liquid CO_2. A test for the complete removal of ethanol is to place a clean sheet of paper at the exhaust hose after it begins to spit out solid CO_2. If there is no wet spot after the CO_2 hits the paper then all the ethanol is gone. Once the ethanol is removed, the chamber is sealed by closing all the needle valves and the heating element is turned on. This will increase the pressure and temperature to bring the CO_2 to a region of the phase diagram beyond the critical point. If

the chamber was initially completely filled with liquid CO_2 increasing the temperature will greatly increase the pressure to dangerous levels (maybe to higher than 2000 PSI). A relief valve is installed in the critical point dryer to limit the pressure to 1300 PSI, which is high enough to go around the critical point. After the relief valve ceases to relieve the pressure, the temperature is kept constant at about 39° C and the exhaust valve is used to slowly reduce the pressure over a period of about 5 minutes to bring the sample safely to 1 atmosphere. The sample is now ready for wirebonding and characterization.

3.11 Growing Tips on Cantilevers

With the help of William Kaminsky, an undergraduate who has done an excellent job in the lab, we have developed a method for growing carbon nano-structures using the scanning electron microscope. We have used this method to fabricate tips for scanning probe microscope cantilevers. The process, developed by Paul Hansma [Walters et al. (1996)], involves first coating a wafer with a thin layer of paraffin and then using an electron beam to change the chemical composition of the paraffin and deposit material in the shape of a tip. For an extensive treatment of this method including a relatively complete report of growth results as a function of SEM beam parameters I refer the interested reader to Bill Kaminsky's Physics 90r paper. Below I will simply state general trends and present the parameters used for tip deposition on our small cantilevers.

After the cantilever has been laterally outlined using the SEM, the underlying layer of AlAs has been exposed around the cantilever, and the resist is removed, the cantilever is ready for tip deposition. We first prepare a paraffin solution by dissolving 2 g of paraffin (in the form of prills) in 100 ml of Xylenes. Large undissolved particles are removed from this solution by allowing it to pass through filter paper. The sample is dipped in the solution and dry nitrogen is gently blown over the chip leaving a thin layer of solution over the area where the tip is to be grown. After allowing the solvent to dry under a 100 Watt

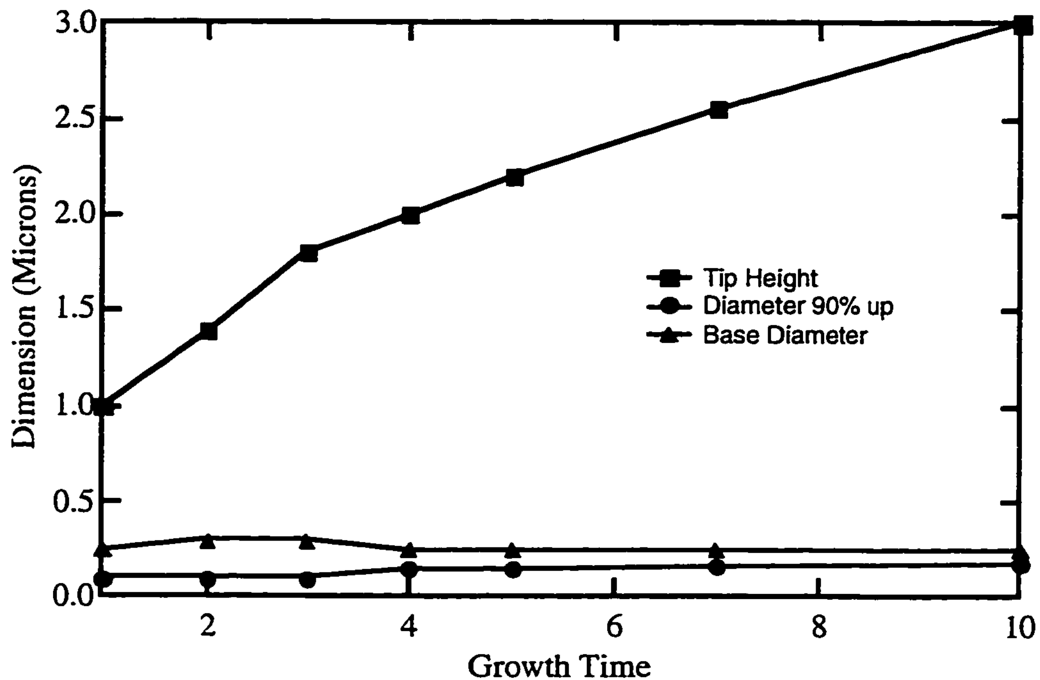


Figure 3.12 Tip dimension verses growth time. Squares are the tip height, triangles are the base diameter, and circles are the tip diameter measured up 90% of the height.

light bulb for about one hour, the chip is mounted on an SEM mount using carbon paint, silver paint flecks are applied to aid focusing, and the sample is placed in the SEM. The silver paint flecks provide small features on which the focus and stigmator settings on the SEM are tuned. The SEM is then set to the BUP mode, which displays the image plus adjustable crosshairs. Using the lowest beam current, the cantilever is found, the magnification is increased to 40,000, and the crosshairs are placed on the desired location for the tip. The SEM is then set to spot mode (SPT) mode causing the beam to rest near the crosshairs for the desired length of time. Before growing the actual tip, a test tip should be grown to determine the exact location of the beam with respect to the crosshairs.

I have found that the best conditions for growing tips on 3 μm x 2 μm cantilevers are the following: working distance 8mm, beam current 3 pA, accelerating voltage 15 kV, and growth time 105 seconds. The working distance and beam current are chosen to produce the smallest base diameter; a small working distance and low beam current result

in a small electron beam diameter leading to a correspondingly small tip base size. The accelerating voltage is chosen to reduce the effect of the beam on the paraffin surrounding the tip; higher accelerating voltages bake on the surrounding paraffin and make it very difficult to remove. The growth time of 105 seconds produces a tip about 1.3 μm high with a 200 nm base diameter. Figure 3.12 shows some relevant tip dimensions as a function of growth time. The base diameters and the diameters measured at 90% of the tip are roughly independent of growth time after the first minute while the height grows in a piecewise linear fashion, or maybe with a square root dependence on time. These trends indicate that growth takes place only at the region where the electron beam is contacting the tip.

After the tip has been grown, the carbon paint is removed from the sample by placing it in acetone for 30 seconds followed by 30 more seconds in acetone and ultrasound. Next the residual paraffin is removed by soaking the sample in Hexanes for 1 minute followed by ultrasound for 30 seconds. Hexanes quickly dissolve the paraffin but do not affect the tip because of its change in chemical composition. There is usually a small ring of undissolved carbonaceous material with a radius of about 2 μm surrounding the tip. The only effective way I have found to remove this is by using an oxygen plasma reactive ion etch. Care should be taken before etching to completely clean the RIE chamber with isopropanol and Scotchbrite to insure a reproducible etch rate. The plasma parameters that I've used are Power = 9 W, DC bias = -250, Flow rate of O_2 = 50 sccm, pressure = 70 mT. The sample is exposed to this plasma for about 1 minute then removed from the RIE and observed with the optical microscope where the radius of the ring can be measured. A total of a few minutes in the plasma may be required to remove the surrounding material. Because the pressure of the RIE is relatively high, it will etch isotropically and will sharpen the tip while removing the baked-on paraffin ring. Care should be taken to make sure that the tip is not totally etched away before removing the surrounding paraffin. For this reason it is necessary to keep the ring as small as possible

Figure 3.13 Three-dimensional electron beam deposited structures grown on a GaAs substrate coated with paraffin. Left: bridge structure that may be useful in measuring the conductivity of the deposited material. Right: EBD tip with a diagonal extension that may be useful for imaging sidewalls with an SPM. The structures and photographs were made by William Kaminsky.

by using low accelerator voltages and by limiting the time the electron beam sweeps across the area surrounding the tip.

This technique has been used not only to grow single pillar-like structures but also to grow three-dimensional structures. By first growing a pillar and then tilting the sample stage and growing another pillar on the top of the first, an armed structure like that seen on the right side of figure 3.13 can be grown. A tip of this shape may be used to image sidewalls using an SPM. A simple extension of this technique makes possible the growth of bridges as seen in the work by Koops [Koops et al. (1993)] and on the left side of Figure 3.12. It would be interesting to measure the resistivity of this material and experiment with different kinds of doping techniques developed for organic semiconductors.

CHAPTER 4

FIELD-EFFECT TRANSISTORS AS STRAIN SENSORS

This chapter describes the fabrication process for field-effect transistors, the characterization of these transistors, and the experiments we performed to measure transistor strain sensitivity at T = 10 K and at T = 77 K. Transistor characteristics such as noise performance, transconductance and drain characteristics are presented. We then describe the method used to apply a known strain to the transistor. Two effects in GaAs that couple strain to electronic charge density are the deformation potential and the piezoelectric effect. We find that the piezoelectric effect can account for the strain response of the FET. The final part of this chapter describes strain sensing at higher temperatures by presenting data from a strain sensing experiment T = 77 K.

4.0 Background and experiment overview

Gallium arsenide micro-electromechanical systems (MEMS) provide a novel environment for studying new physical phenomenon [Tighe et al. (1997)] and offer new possibilities for device applications [Uenishi et al. (1995); Zhang et al. (1992); Hjort et al. (1990)]. Sensing systems for either strain or position are central to the functionality of many (MEMS). The most widely used methods for strain sensing include resonance

frequency monitoring, piezoresistive and piezoelectric measurements. Position can be monitored optically or by monitoring position dependent capacitance or thermal conductivity. This chapter will describe the fabrication and characterization of strain-sensing FETs for integrated sensors in GaAs/AlGaAs MEMS. It is known that the piezoelectric properties of GaAs affect FET parameters [Asbeck et al. (1984); Chang et al. (1984); Onodera et al. (1985)]. We exploit this dependence using low noise FETs to make strain sensors capable of sensing volume or dilatational strains $\varepsilon < 2 \times 10^{-9}/\sqrt{Hz}$.

The idea of this experiment is to fabricate a field-effect transistor, characterize it and measure its response to a known strain. To do this we mount the chip containing the FET on a piezoelectric bimorph and use the bimorph to drive the sample through its mechanical resonance thus applying a variable strain to the FET. After characterizing the FET and measuring its response to a known strain, the strain sensitivity of the FET was calculated. This sensitivity determines its usefulness as a force or displacement sensor for nano-electromechanical systems.

4.1 Field-Effect Transistor Fabrication

Field-effect transistors were fabricated on large sample with dimensions 2.5 mm x 15 mm chosen to give a lower mechanical resonance frequency < 5 kHz. This chip was cleaved from a GaAs/AlGaAs heterostructure containing a near-surface two-dimensional electron gas (2DEG). The 2DEG, with sheet density $2 \times 10^{11}/cm^2$ and mobility $\mu = 1.5 \times 10^5$ cm^2/V-sec at 4.2 K, is confined by a 200 Å square well beginning 520 Å beneath the surface. The wafer (labeled 940922d) has a composition and conduction band profile shown in Figure 3.1.

Fabrication proceeded in the following steps. Ohmic contacts were formed by first spinning a bilayer of resist 3,100 Å thick onto the sample. The bilayer was composed of a 4% 496 K molecular weight resist layer followed by a 2% 950 K layer both spun at 4,000

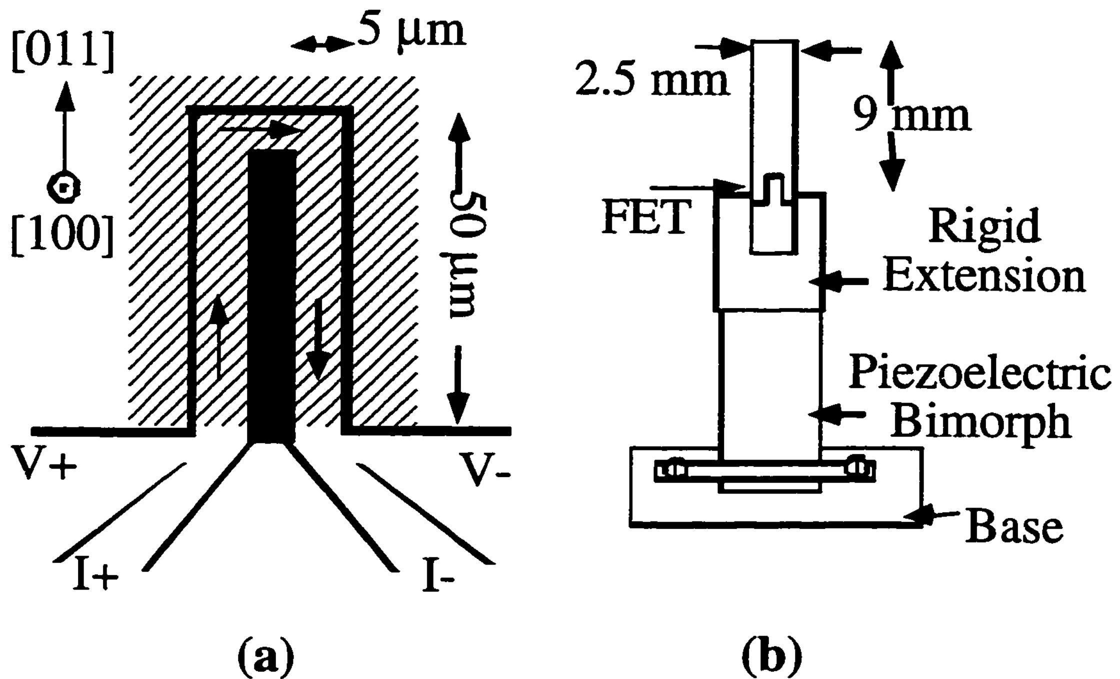


Figure 4.1 (a) Schematic of field-effect transistor (FET) geometry. Dark lines are etch trenches, diagonal line pattern represents top gate, arrows indicate current path through channel. The [100] direction is out of the page and [011] is indicated. (b) Schematic of mounting system for FET substrate.

RPM. The contacts were patterned to measure the FET channel resistance using a four-probe measurement configuration with multiple pads for each contact to ensure successful wire bonding. Both the drain and source contacts and alignment markers were patterned using the SEM and Au, Ni, and Ge layers were deposited and annealed. Next, the FET channel was formed. The resist mask for this step consisted of a PMMA monolayer 1,100 Å thick composed of 2% 950 K resist spun at 4,000 RPM. After lithography, samples were dipped in a 1:5 solution of ammonium hydroxide and water followed by a dip in a 1:10 solution of citric acid (mixed 1:1 by weight with distilled water) and 30% hydrogen peroxide solution until the etch depth was about 1,000 Å. The final lithography step was to produce a Schottky gate over the channel. We spun a 9,000 Å bilayer of resist composed of 4% 496 K resist spun at 3,000 RPM followed by a 6% 950 K resist layer spun at 6,000 RPM. We then evaporated 200 Å Cr followed by 2,000 Å Au; the

thickness was chosen to ensure gate continuity across the etch trenches. Figure 4.1(a) shows a schematic of the FET. The sample was then mounted, and wirebonds were used to attach the contacts to the external circuit

4.2 Experimental Setup

Figure 4.1(b) illustrates how strain was applied to the field-effect transistor. The chip, 2.5 mm x 14 mm, containing the FET was mounted on a piezoelectric bimorph, which was used to drive the chip through its mechanical resonant frequency. The FET was placed in the region of maximum strain near the clamped end of the chip as indicated. An aluminum piece reinforced with small Macor block served as both a rigid extension to prevent deformation of the bimorph from straining the sample and as a ground plane to isolate the sample from the relatively large voltages applied to the bimorph. The FET/bimorph assembly was mounted in vacuum inside a thermal shield attached to the cold plate of an Infrared Labs liquid helium Dewar with an opening in the shield to allow optical access to the entire chip. The sample temperature was ~ 10 K due to heating from black body radiation through the optical access window located 7 cm away.

4.3 Transistor Characteristics

Figure 4.2 shows the circuit used to measure the field-effect transistor characteristics. The diagram includes the parasitic capacitance from the Dewar leads and external amplifiers. In order to characterize the FET we measure FET noise, the small signal drain-source resistance r_{DS}, and the transconductance g_m. These parameters will give us the dimensionless voltage gain of the amplifier given by $A_v = g_m(R_D \| r_{DS})$ and its output impedance $R_D \| r_{DS}$. The amplifier input impedance is given by the gate channel resistance in parallel with the gate capacitance of 1 pF. For noise and strain effect measurements, we

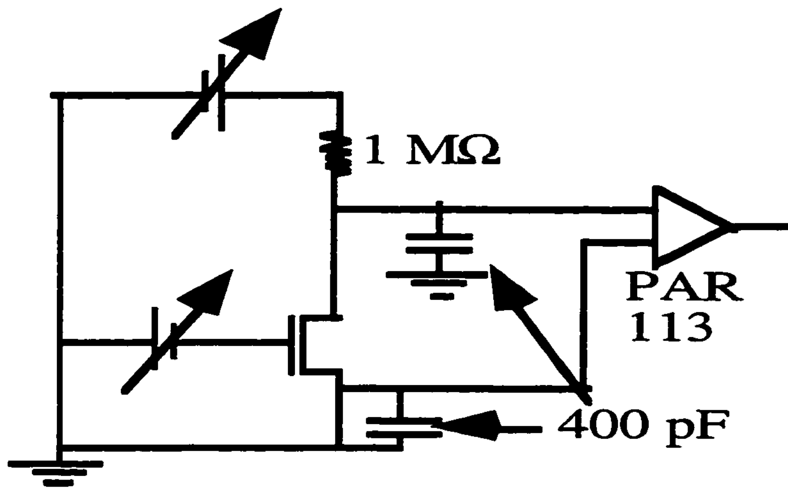


Figure 4.2 Schematic of circuit used to characterize the FET and measure its strain response. The Dewar lead capacitances are included.

choose an FET bias point and monitor small deviations in drain-source voltages, v_{DS}, about that point. These deviations are constrained by the drain resistor to a load line represented by the dashed line in Figure 4.3.

Figure 4.3 shows the measured drain characteristics for the field-effect transistor at T ~ 10 K. The transistor operates with low noise in the saturation region and displays a typical small-signal drain-to-source resistance r_{DS} ~ 10 MΩ and transconductance g_m ~100 μS which results in a transconductance per unit gate width of 20 mS/mm. This is small compared to the best values of ~700 mS/mm found in commercial FETs [Chang, (1994)] due to the long, narrow channel of our device. In contrast to the result of Mar et al. (1994) who fabricated transistors from a single heterointerface, no carrier heating effects were observed even for extreme pinch off values (V_{GS} = -150 mV and V_{DS} = 6 V) indicating that the electrons are strongly confined by the square well structure.

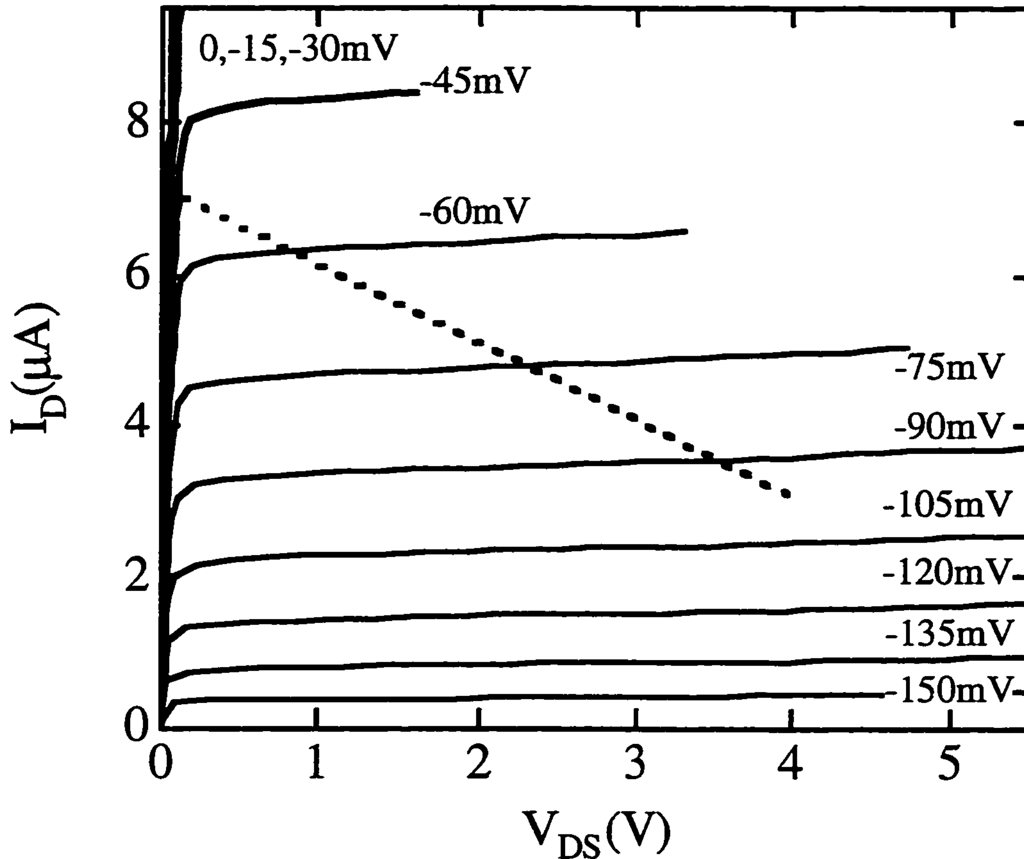


Figure 4.3 Family of source-drain characteristics taken at T~ 10 K. Voltages indicate gate-source voltage, V_{GS}. The dotted line is a load line indicating the constraints of the external circuit.

Figure 4.4 shows a plot of normalized channel conductance G versus gate voltage V_{GS}. The conductance changed by five orders of magnitude with V_{GS} from its zero gate voltage value $G_o = 2.5$ mS. The small magnitude of the pinch-off voltage ($V_{po} = -170$ mV) gives excellent sensitivity while the smooth, constant curvature indicates little parallel conduction.

The measured gain and frequency response are in accord with simple field-effect transistor models [Schilling, (1979)]. At a typical operating point ($V_{GS} = -85$ mV and $I_D = 3.8$ μA) the dimensionless voltage gain is $A_v = 70$. This gain was found to vary with current as the transconductance does, $A_v \propto g_m \propto I_D^{1/2}$ as expected. Dewar lead

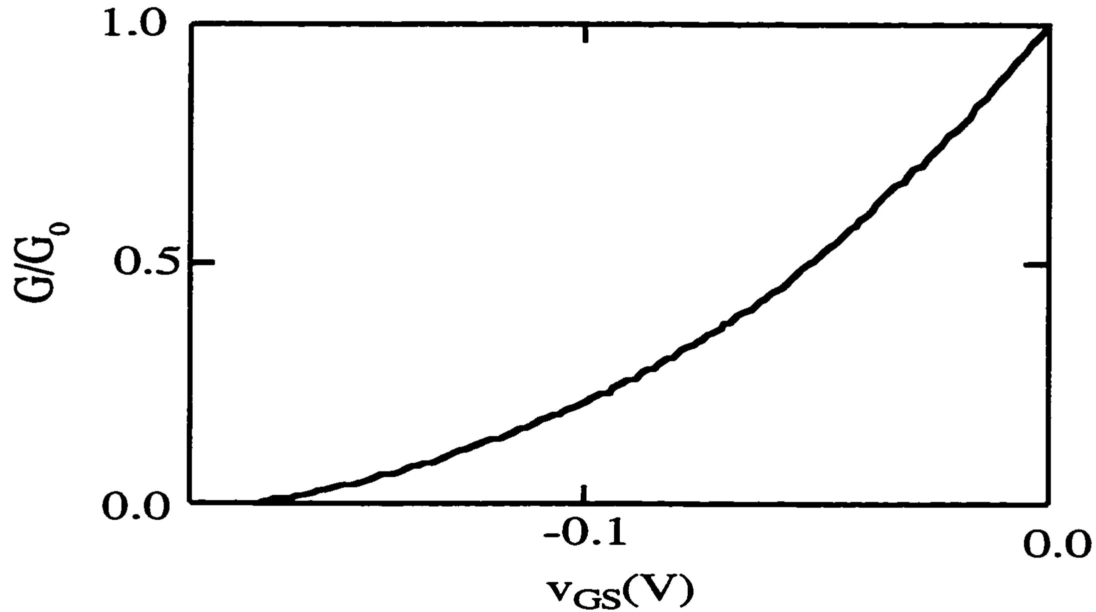


Figure 4.4 Cutoff graph of channel conductance G normalized to its zero gate voltage value G_o = 2.5 mS. The pinch-off voltage is V_{po} = -170 mV.

capacitance ~ 400 pF combined with the amplifier output impedance of $R_D \| r_{DS}$ ~ 0.9 MΩ caused the output signal to roll-off above a 3 dB point of 400 Hz. When we compensated for this roll-off, we measured a constant transconductance as the frequency was varied up to 100 kHz limited by the measurement electronics. A figure of merit for the transistor speed given by C_G/g_m, where C_G is the gate/channel capacitance, indicates an intrinsic rolloff frequency of 16 MHz for the geometry of figure 4.2. Much higher operating frequencies can be obtained using FETs with shorter and wider channels.

The noise of the field effect transistor was measured using a circuit similar to that shown in figure 4.2. The output of the PAR 113 was connected to an HP 3561a signal analyzer. Reliable noise measurements of the field effect transistor require the elimination or reduction of environmental noise. During measurements we power all the amplifiers with internal batteries and make sure that the circuit is connected to ground by only one point to avoid ground loops. We then try to eliminate all periodic noise sources by turning off various unused electrical components. Some common noise sources, their associated

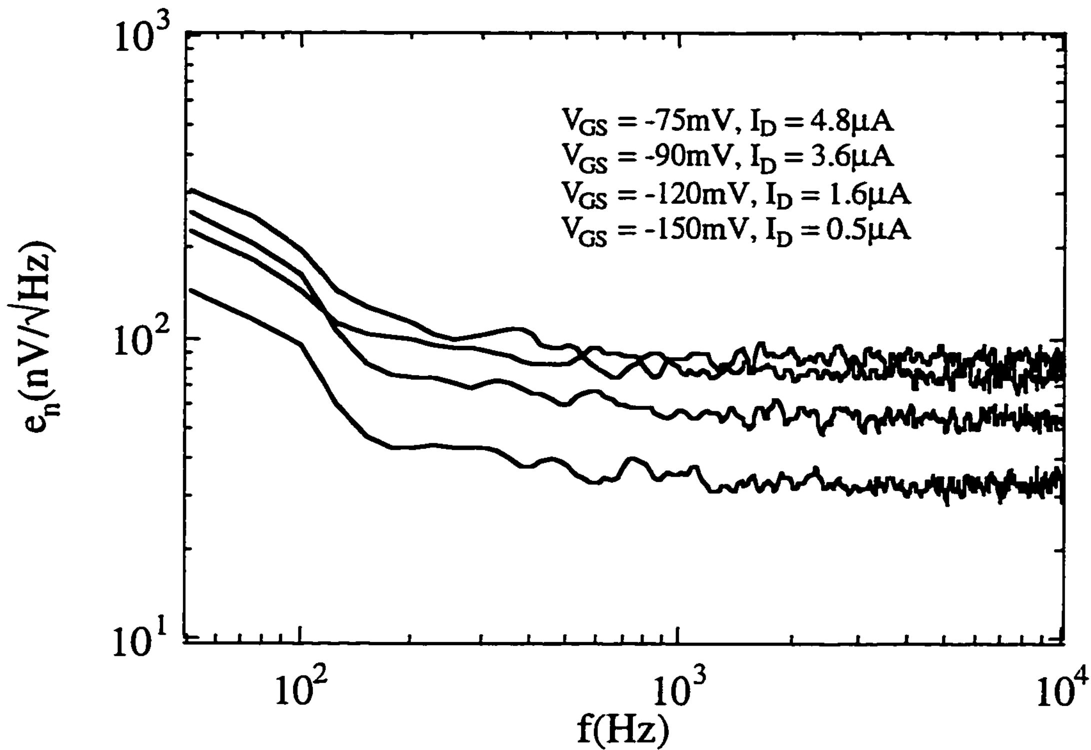


Figure 4.5 Family of noise spectra taken at T = 10 K corrected for RC rolloff of the external circuit. The lowest white noise value corresponds to a charge noise of 0.2 e/√Hz. The 1/*f* noise corner is < 300 Hz.

frequencies and the steps taken to reduce their effect are the following: building vibrations, low frequency noise (~12 Hz), make measurements at night when there is little activity in the building and don't move while taking data; line frequency and harmonics, 60 Hz and harmonics, turn off unused electronic equipment, eliminate ground loops and reduce flux enclosed in the circuit by twisting the leads together (in some cases flux cancellation can be done by taping the leads to a board in the configuration that reduces or cancels out magnetic pickup); bimorph resonance frequency, 400 Hz, don't tap table or talk during measurements; hand held Fluke multimeters, 1 to 2 kHz, switch fluke out of circuit while taking measurement; HP3561a monitor, 36 kHz, move signal analyzer far away from experiment; computer monitor, 50 kHz, turn off monitors during measurements. Noise reduction is a matter of trial and error; ground loops can be hidden and sometimes the ground itself is noisy (especially if the ground is shared by a computer). Thus it may be

advantageous to isolate the circuit ground from the measurement electronics.

Figure 4.5 shows measured spectra for voltage noise e_n referred to the input of the field-effect transistor. The noise is characterized by a flat spectrum at high frequencies with a low 1/f noise corner of 300 Hz. In the saturation region the magnitude of the noise e_n is independent of drain source voltage V_{DS} for a given gate-source voltage V_{GS} but increases with increasing channel current as $e_n^2 \propto I_D$. The noise contribution from the external circuit is dominated by a white noise level of 20 nV/$\sqrt{\text{Hz}}$ from the ramper box voltage source used to apply a voltage to the gate. Noise from the PAR 113 amplifier is negligible for source resistances of ~ 1 MΩ. The lowest noise occurs for V_{GS} = -150 mV where the white noise level corresponds to a gate charge noise $\delta q_g = e_n C_g < 0.2$ e/$\sqrt{\text{Hz}}$.

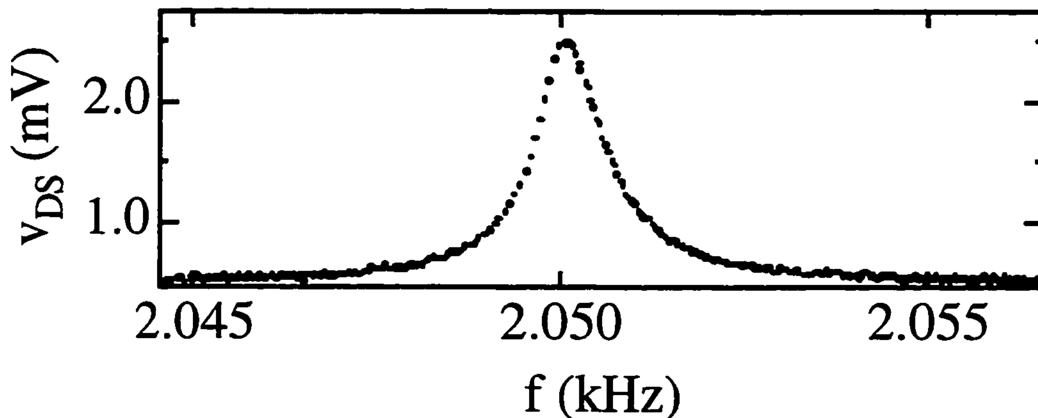


Figure 4.6 Small signal drain-source voltage v_{DS} for an operating point of V_{GS} = -85 mV and I_D = 3.8 μA as FET substrate is driven through its lowest mechanical resonance.

4.4 Measuring Strain

The field-effect transistor was strained by applying a variable frequency voltage (0.25 V_{pp}) to the bimorph to drive the chip through its lowest mechanical resonance. Figure 4.6 shows the measured small signal response v_{DS} of the FET for V_{GS} = -85 mV and I_D = 3.8 μA about the sharp (Q = 2000) mechanical resonance of the chip.

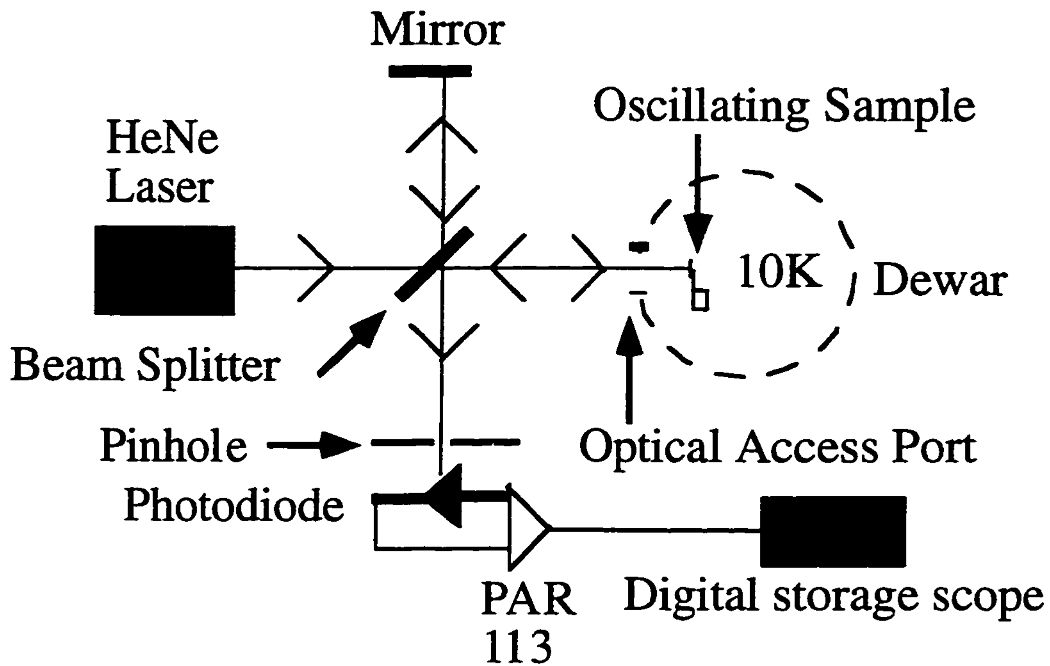


Figure 4.7 Schematic of Michelson interferometer setup used to measure the chip deflection at resonance.

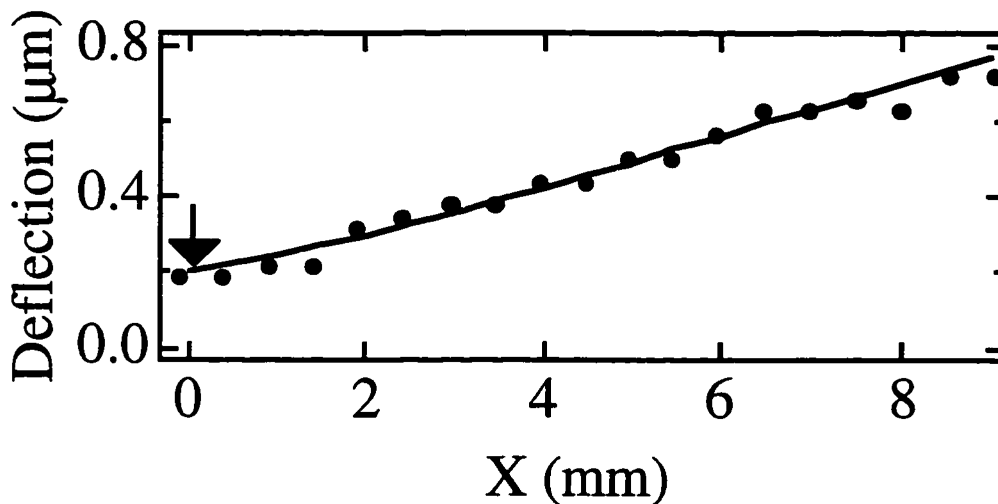


Figure 4.8 Measured deflection as a function of position along the length of the GaAs chip at its lowest mechanical resonance. The arrow indicates the position of the FET and the free end of the chip is at 9 mm. The line indicates a fit to the data.

4.4.1 Experimental Apparatus

The strain at this resonance was measured using a Michelson interferometer operating through an optical access port in the Dewar. Figure 4.7 shows a diagram of the interferometer setup. The beam from a 6 mW helium neon laser was split to form the two arms of the interferometer. One beam was reflected from a mirror bolted to the optical table while the other beam passed through a quartz optical access port of the Dewar and was reflected from the surface of the GaAs chip. The Dewar was placed on a milling machine table where it could be easily moved by the linear actuators to slide the Dewar/chip along the interferometer arm and measure the deflection at different points on the chip. The beam was then recombined and projected onto a photodiode through a pinhole punched in a piece of copper foil. The pinhole was smaller than the width of the interferometer fringes and thus provided a large contrast in the photodiode light level. The photodiode voltage was amplified by a PAR 113 amplifier and monitored using a digital storage scope. The number of fringes in one cycle could be determined by looking for a repeating pattern in the photodiode signal. The fringes with the slowest variation correspond to the turnaround points of the chip's motion. One could make this point a peak or valley by adjusting the dc offset of the bimorph and then could count fringes to an accuracy of 1/4 fringe. The wavelength for the helium neon laser is $\lambda = 630$ nm and a fringe counting accuracy of 1/4 fringe will give a displacement resolution for this technique of $\lambda/8 = 80$ nm.

4.4.2 Determining The Strain at the FET

Figure 4.8 shows the amplitude of deflection along the entire length of the chip measured using the Michelson interferometer; the arrow indicates the position of the field-effect transistor. We proceed to describe two methods used to determine the strain in the location of the FET channel. The first one involves finding the functional form describing

the shape of the driven beam, determining the parameters of that function, and computing the strain. The second one involves making an approximation that the beam is a rigid body in translational and rotational motion and calculating the stress about the cross section at the FET channel required to maintain this motion. We compare the results from these two methods.

In chapter 2 we derived the equation describing the amplitude of deflection of a vibrating cantilever beam

$$u(z) = A\cos(\kappa z) + B\sin(\kappa z) + C\cosh(\kappa z) + D\sinh(\kappa z) \qquad (4.1)$$

Where

$$\kappa = \frac{\omega^2 \rho S}{EI}. \qquad (4.2)$$

This solution has four unknown coefficients that we will solve for by supplying four pieces of information. The first two come from the two boundary conditions of zero torque and zero force at the free end of the cantilever. Thus,

$$F(L) = \left.\frac{d^3u}{dz^3}\right|_{z=L} = 0 \text{ and } \tau(L) = \left.\frac{d^2u}{dz^2}\right|_{z=L} = 0. \qquad (4.3 \text{ and } 4.4)$$

The third piece of information is obtained from the measured amplitude of oscillation at the end where the chip is attached to the bimorph. We cannot use the slope $\left(\frac{du(z)}{dz}\right)_{z=0}$ of the chip at the end of the bimorph for the fourth piece of information because the bimorph is being driven at frequencies above its first mechanical resonance of ~ 400 Hz and therefore may be unpredictably deforming. Thus, the final piece of information is the measured vibration amplitude at the end of the chip. The coefficients are calculated and the resulting expression plotted as the solid line in figure 4.8.

Once the coefficients are known, the uniaxial strain at any point distance z along the length of the lever and distance x above or below the center of the cantilever in the plane of bending is given by

$$\varepsilon_u(x,z) = x\frac{d^2u(z)}{dz^2} = x\kappa^2[-A\cos(\kappa z) - B\sin(\kappa z) + C\cosh(\kappa z) + D\sinh(\kappa z)] \quad (4.5)$$

Using the calculated coefficients gives a uniaxial strain at the channel of 2×10^{-6} which corresponds to a stress of 2.4×10^5 N/m^2.

The validity of this number can be supported by a calculation based on the following simple approximation. Because the deflection of the beam is very small, we can approximate it as a rigid body translating a distance d, the motion of the end of the bimorph, and rotating about the bimorph end with an amplitude mL where m is the slope at maximum displacement given by $(u(L)_{max} - d)/L$ where $u(L)_{max}$ is the measured maximum displacement at the cantilever end and L is the length of the beam. Thus, its amplitude $u(z,t)$ can be described by

$$u(z,t) = (mz + d)\cos(\omega t + \delta) \quad (4.6)$$

Newton's second law requires that a force $F(z)$ given by

$$F(z) = \rho S\omega^2(mz + d) \quad (4.7)$$

be supplied to maintain this motion. This force is supplied by a torque at the base of the cantilever which is caused by a stress, $\sigma(x)$, on the cross section that we assume has a linear distribution with a value of zero at the center of the cantilever cross section. Integrating $F(z)z$ along the length of the lever gives the total torque τ on the cross section at the base of the lever. This torque can also be calculated by

$$\tau = b \int_{-\frac{t}{2}}^{\frac{t}{2}} \sigma(x) x dx = \frac{1}{6} \sigma_o b t^2. \qquad (4.8)$$

Equating these two torques allows us to approximate the stress in the region of the channel to be 2.4 x 10^5 N/m^2 corresponding to a uniaxial strain of 2 x 10^{-6} and agreeing very well with the results derived using the functional form.

Under stress, GaAs will respond by a strain in the direction of the stress plus strain of opposite sign in the two directions perpendicular to the stress [McClintock (1965)]. The magnitude of the parallel response is given by Young's modulus while the perpendicular response is given by Young's modulus and Poisson's ratio ν. For a stress in the z direction on the z face, σ_{zz}, the resulting strains are related to one another by

$$\varepsilon_{xx} = \varepsilon_{yy} = -\nu \varepsilon_{zz} \quad ; \quad \nu = 0.31. \qquad (4.9)$$

Thus, for the measured stress on our FET channel of 2.4 x 10^5 N/m^2 the uniaxial strain is 2.4 x 10^5 N/m^2 and the volume or dilatational strain is $\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz} = 7 \times 10^{-7}$. Now we are ready to calculate the electronic effects of this strain.

4.5 Electronic Effects

Two mechanisms that provide an electronic response to strain in GaAs are the deformation potential and the piezoelectric effect. Both couple strain to a change in the number of electrons in the FET channel. At the mechanical resonance we measure a small signal FET response, v_{DS}, corresponding to a change in amplitude of 250 electrons on the gate. We will now explore the magnitudes of the two electronic strain effects to determine which effect is dominant.

4.5.1 The Deformation Potential

The deformation potential is the change in semiconductor band energy in response to strain. For the conduction band in GaAs this change dE_c is given by [Blakemore, (1987)]

$$dE_c = a(\varepsilon_{xx} + \varepsilon_{yy} + \varepsilon_{zz}) = a\varepsilon_{ii} \tag{4.10}$$

where a is the hydrostatic deformation potential which has a value between –7 and -9 eV [Inspec Data Review, (1990)]. When a region is strained, its local conduction band energy will be shifted and electrons from unstrained regions will move to equalize the chemical potential. Figure 4.9 illustrates how we can model this effect. Shown in this diagram are two capacitors with a common lower plate representing the 2DEG. The capacitors can be used to alter the local conduction band energy in the 2DEG. The left capacitor represents the source lead of the FET that is at a voltage V_S with respect to ground. This source lead is modeled as an infinite capacitor implying that it can supply charge with no resulting voltage change. The capacitor on the right represents the strained region of the FET channel and is at a potential V_{GS} above the

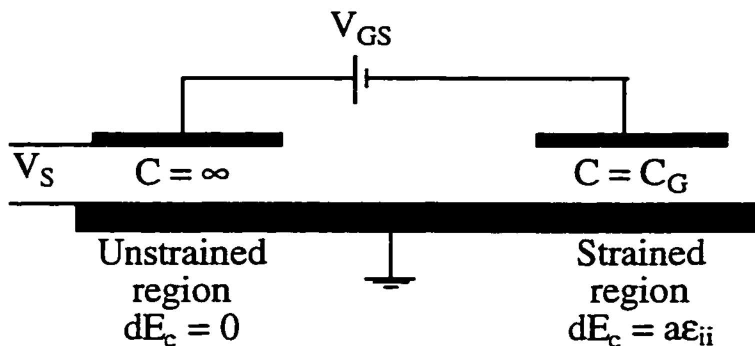


Figure 4.9 Model for calculating magnitude of the change in charge due to the deformation potential. The lower grounded bar represents the 2DEG. The left capacitor represents the unstrained source lead. The right capacitor represents the strained region under the FET gate under a gate bias V_{GS}.

source. This region has a gate capacitance C_G and will have its conduction band energy shifted an amount dE_c by strain. Assuming the 2DEG is degenerate and therefore the entropy is small, the electronic Helmholtz free energy F(T, V, N) for the strained region is

$$F(T,V,N) = -Ne(V_S + V_{GS} + dE_c) + \frac{(Ne)^2}{2C_G} + E_{quantum} + Constant \qquad (4.11)$$

Where N is the number of electrons removed from the strained region, e is the electronic charge, $E_{quantum}$ is the energy required to fill up the quantum states in the 2DEG,and the constant is a term independent of N. The quantum energy can be written as

$$E_{quantum} = \int_{-\infty}^{\infty} g(\varepsilon) f(\varepsilon) \varepsilon d\varepsilon \qquad (4.12)$$

Where ε is the energy of a state,$g(\varepsilon)$ is the two dimensional density of states, and $f(\varepsilon)$ is the Fermi-Dirac distribution function. Differentiating the free energy F with respect to number gives the chemical potential of the strained region

$$\mu = \left(\frac{\partial F}{\partial N}\right)_{T,V} = -e(V_S + V_{GS} + dE_c) + n_S e^2 \left(\frac{1}{C_G/A} + \frac{1}{e^2 D}\right) \qquad (4.13)$$

where n_s is the 2DEG number density, A is the area of the FET gate, and D is the two-dimensional density of states. The last term in 4.13, the one involving D, accounts for the energy required to change the Fermi level. This quantum term is found to be 25 times smaller than the term involving the geometrical capacitance (A/C_G) and is therefore neglected in our calculation. By setting the chemical potential of the strained region and unstrained regions equal we can calculate the number ΔN of electrons exchanged with the strained region for a given strain ε_{ii}

$$\Delta N = \frac{dE_c C_G}{e} = \frac{a C_G}{e}\varepsilon_{ii} \tag{4.14}$$

For a measured volume strain of 7 x 10^{-7} and a gate capacitance of 1 pF, the deformation potential alone will result in a change in number of gate electrons of 35. This is a factor of 7 smaller than our measured value indicating that the deformation potential cannot account for the full effect we observe.

4.5.2 The Piezoelectric Effect

A material is piezoelectric if a strain or deformation can induce an electronic polarization in it. This effect is only found in crystals composed of more than one element and lacking a center of inversion symmetry. One can see why a material with a center of symmetry cannot be piezoelectric if we imagine a material having a center of symmetry, under stress, with an induced polarization. Under inversion of the entire system, the crystal remains the same, the stress remains the same, and the polarization reverses direction. The only way this can be true is if the polarization for this crystal is zero. Since GaAs lacks an inversion center, it can be and is piezoelectric. GaAs is one of the weaker piezoelectric materials having piezoelectric constants of similar magnitude to that of quartz but about 100 times smaller than that found in good piezoelectrics like the ceramic PZT. Excellent, detailed treatments of the piezoelectric effect can be found in the books by Ikeda (1984), Cady (1964), and Nye (1957).

A physical illustration of how the piezoelectric effect works in GaAs can be seen by looking at a GaAs unit cell in figure 4.10 [Blakemore, (1987)]. The clear and shaded circles represent different atoms each of which share a different charge. A force applied along the two cube edges indicated by the arrows will cause the upper two white atoms to move down due to a compressive strain. The lower two atoms will also move down due to

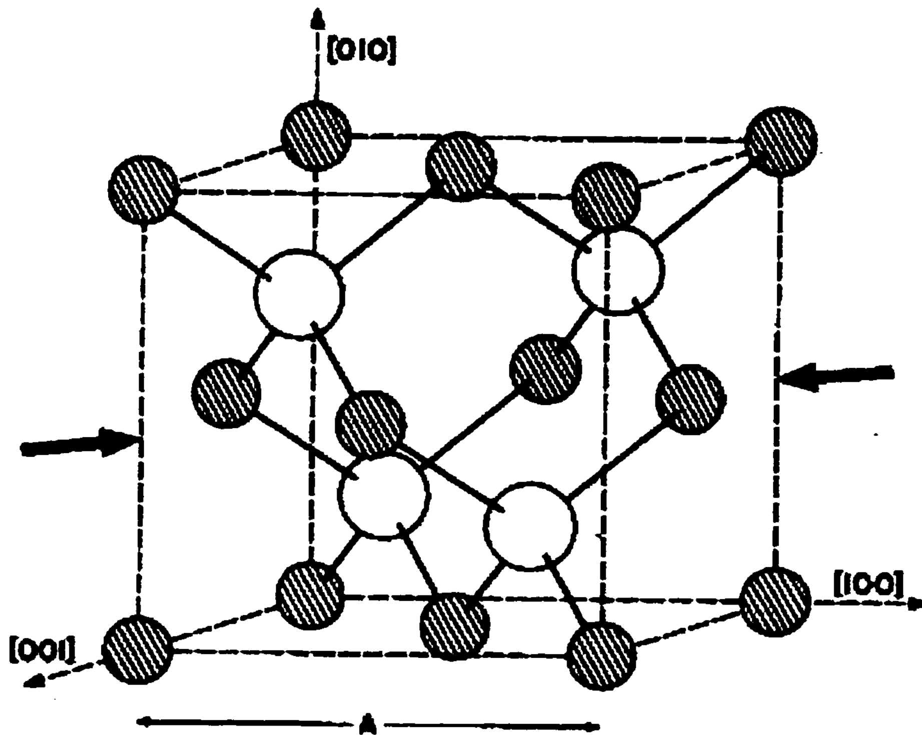


Figure 4.10 GaAs unit cell.

an extension in the direction perpendicular to the applied force accounted for by Poisson's ratio. Thus, all white atoms move down with respect to the shaded atoms causing the unit cell to develop an electric dipole moment. A force applied to a face will move one set of white atoms up and the other set down and thereby cause no net electric dipole moment.

As seen from the example above, the anisotropic nature of crystals complicates the description of piezoelectric properties. A stress in one direction will cause a polarization while a stress in another causes none. Also a stress in any direction, whether shear or uniaxial, can affect the polarization in any given direction. Thus, to determine the polarization, one must relate each polarization component to every element of the stress tensor describing the applied stress. The stress tensor has 6 independent elements therefore 3 x 6 = 18 parameters are needed to describe the piezoelectric effect. For zinc-blend

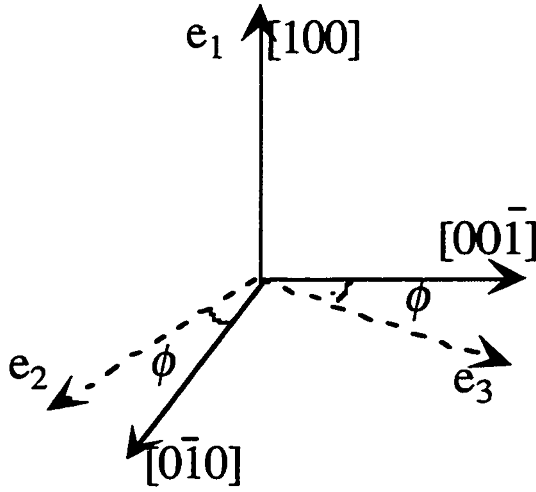


Figure 4.11 Diagram showing GaAs crystal axis and the axes of the applied stress.

crystals, like GaAs, symmetry reduces the number of independent components to 4 [Nye, (1957)]. Generally, all the piezoelectric information can be embodied in the third rank piezoelectric tensor that is used to relate the first rank polarization tensor with the second rank stress tensor. In subscript notation this is described by

$$P_i = d_{ijk}\sigma_{jk} \tag{4.15}$$

where P_i is the component of polarization in the i direction, σ_{jk} represents the components of the stress tensor and d_{ijk} represents the components of the piezoelectric tensor for GaAs. Repeated indices are summed over.

The GaAs piezoelectric tensor for stress applied along the e_1,e_2, e_3 axis defined with respect to the GaAs crystal directions in Figure 4.11 is [Fricke, (1991)]

$$d_{[100]} = d_{14}\begin{pmatrix} 0 & \delta_1 & -\delta_1 & \delta_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & \delta_2 & 2\delta_1 \\ 0 & 0 & 0 & 0 & -2\delta_1 & \delta_2 \end{pmatrix} \tag{4.16}$$

where $\delta_1 = \cos\phi\sin\phi$ and $\delta_2 = \cos^2\phi - \sin^2\phi$. In this tensor each row is associated with a component of the polarization vector. Each colum is assciated with an independent component of the stress tensor, beginning from left to right these are σ_{11}, σ_{22}, σ_{33}, σ_{23}, σ_{13}, and σ_{12}. For our experiment, we apply stress in the $0\bar{1}1$ direction so we set $\phi = 45°$;

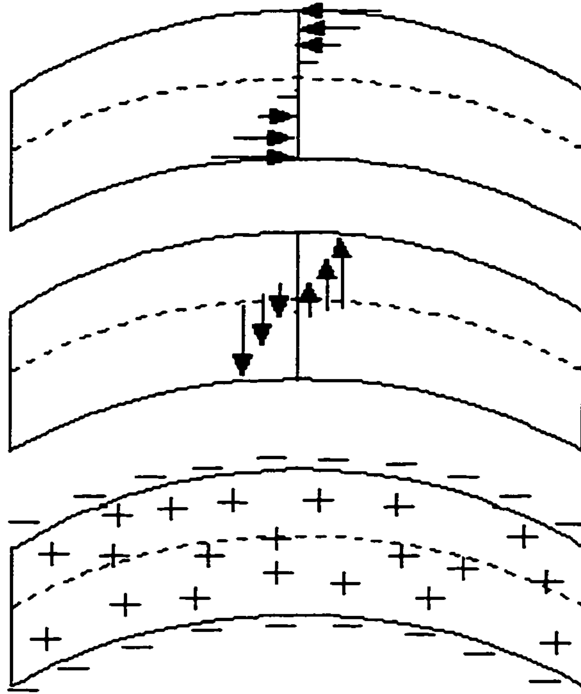


Figure 4.12 (a) Strain distribution in a homogeneous bent beam. The dotted line marks the neutral line. Length of the arrows indicates magnitude of strain. (b) Polarization (c) charge

thus δ_1 = 1/2 and δ_2 = 0. For GaAs d_{14} = -2.7 pC/N while for $Al_xGa_{1-x}As$ d_{14} varies with x as d_{14} = (-2.7-1.13x) pC/N.

To quantitatively predict the magnitude of the electronic response in a two-dimensional electron gas due to the piezoelectric effect in a bending beam, we must first know the stress distribution then derive the polarization and associated bound charge. For small deflections equation (4.5) gives the strain at any point in a vibrating cantilever beam. For cantilevers with symmetric cross sections, a line on the cross section, perpendicular to the plane of bending and midway through the cantilever thickness will have zero strain; this line is called the neutral line. For negative curvature, regions below this line will have a linearly varying positive or compressive strain while regions above this line will show a linearly varying negative or tensile strain. This strain distribution, shown in Figure 4.12a will couple via the d_{12} term in the piezoelectric strain tensor (4.16) to produce a polarization distribution shown in Figure 4.12b. Figure 4.12c shows the resulting bound charge distribution where the volume bound charge is given by $\rho_b = -\nabla \cdot \vec{P}$ and interface bound charge $i_b = \hat{n} \cdot \vec{P}$. For a cantilever beam composed of more than one material, in addition to the volume bound charge induced by the divergence of the polarization, there will be sheets of bound charge induced at every interface having a piezoelectric constant mismatch.

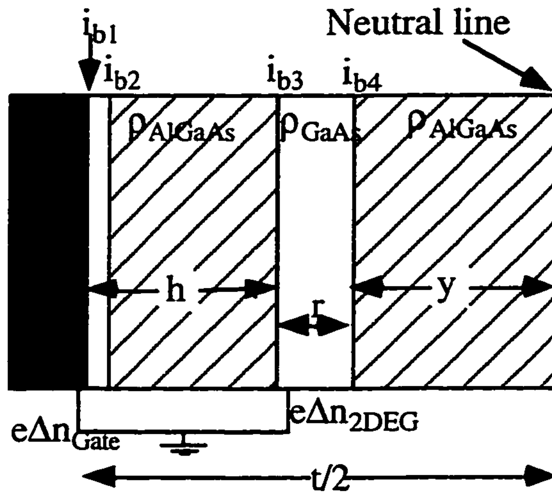


Figure 4. 13 Schematic of half of a cantilever with thickness t showing the 2DEG channel and the resulting induced bound charges. The diagonal lined areas are AlGaAs, the clear areas are GaAs and the shaded area is the gate. The gate and gas are grounded to calculate the screening charge on the 2DEG.

Figure 4.13 shows a diagram of such a multi-layer cantilever structure with thickness t and with a linearly varying strain applied to it. The figure shows half the cantilever, the part containing the 2DEG, from the neutral line where the strain is zero to the gate. The associated strain induced volume ρ and interface i bound charges are shown where ρ_{AlGaAs} or ρ_{GaAs} are the strain induced volume bound charge in the AlGaAs and GaAs regions respectively and i_{b1}, i_{b2}, i_{b3}, i_{b4} are the strain induced charges at the interfaces indicated in the diagram. The gate and 2DEG are both grounded allowing a screening charge $e\Delta n_{Gate}$ to flow to the gate and $e\Delta n_{2DEG}$ to flow into the 2DEG in response to the strain induced charges. In the diagram y is the distance between the well and the neutral line, r is the well width, and h is the distance between the gate and the well.

In order to estimate the strain induced signal, we must calculate the change in electron density in the 2DEG in response to this induced polarization charge. Implicit in this calculation is some assumption about the screening of the polarization by charge outside the well. Such screening will give no measurable signal in response to strain. We propose three screening models and compare the calculated results to the measured response. The first model assumes zero screening by outside well charge and complete screening by electrons in the 2DEG and gate. The second model assumes partial screening by outside well charge, leaving the 2DEG to screen only the induced charge in the quantum well and its two cladding interfaces. The third model, an extreme screening model,

assumes all polarization outside the region occupied by the 2DEG is screened. For the 940922d heterostructure (shown in figure 3.1) the 2DEG has thickness ~ 100 Å [Harris et al. (1989); Katine (1996)] and resides very close to the gate-side interface of the well (see Figure 3.3a). This model assumes the 2DEG screens only the charge induced on this gate-side interface and in half the well.

In the first model, where we assume that no screening takes place outside of the 2DEG, we connect both the FET gate and channel to ground allowing screening charges to freely accumulate in these two areas in response to the bound charge. Charge neutrality indicates that the induced charges on the gate and gas should be related by

$$\Delta n_{2DEG} = -\Delta n_{Gate} \tag{4.17}$$

and similarly the interface and volume bound charges should sum to zero

$$-\int_0^{t/2} \rho(x)dx = i_{b1} + i_{b2} + i_{b3} + i_{b4} \tag{4.18}$$

where $\rho = -\nabla \cdot \vec{P} = -\frac{2\sigma_o d_{12}}{t}$ and $i_{b4} = n \cdot \overrightarrow{P_{AlGaAs}} + n \cdot \overrightarrow{P_{GaAs}} = \sigma_o \frac{2y}{t}(d_{12AlGaAs} - d_{12GaAs})$.

Here σ_o is the maximum stress at the cantilever surface, d_{12} is the row 1 column 2 component of the piezoelectric tensor for the relevant material (either GaAs or AlGaAs as indicated by the subscript). With both gate and 2DEG grounded we integrate the electric field along a line from gate to gas and set this value equal to zero:

$$\int_{2DEG}^{Gate} \vec{E} \cdot d\ell = 0. \tag{4.19}$$

This gives us the screening charge induced in the well $e\Delta n_{2DEG}$

$$e\Delta n_{2DEG} = \frac{2}{3}\sigma_o(1-\frac{h}{t})d_{12,Al_{0.3}Ga_{0.7}As} \quad (4.20)$$

For the second and third models we simply sum up the magnitude of the charge induced in the regions specified by the model. The charge induced in the quantum well and its two cladding interfaces is

$$e\Delta n_{2DEG} = 2\sigma_o d_{12,Al_{0.3}Ga_{0.7}As}\frac{r}{t} \quad (4.21)$$

Similarly, the charge induced in the region occupied by the 2DEG, namely the gate-side interface of the well and half the well, is given by

$$e\Delta n_{2DEG} = \frac{-2\sigma_o}{t}\left[\Delta d\left(\frac{t}{2}-h\right)+\frac{r}{2}d_{12GaAs}\right] \quad (4.22)$$

where $\Delta d = d_{12AlGaAs} - d_{12GaAs}$.

From our interferometer measurements we calculate a stress in the region of the FET of $\sigma_o = 2.4 \times 10^5$ N/m^2 and measure a change of 250 electrons on the gate in response to this stress. Equation (4.20), which assumes that no charge outside of the quantum well screens the piezoelectric polarization, predicts a change of 750 electrons in response to the measured stress. Equation (4.21), which assumes the 2DEG is only affected by charge induced in the well and at the two cladding interfaces, predicts a change in charge of 0.1 electrons. Equation (4.22), the extreme screening model, predicts a signal of 112 electrons.

We gain a little more insight into screening by realizing that the polarization is screened in the dielectric relaxation time given by $\varepsilon\rho$ where ε is the dielectric constant of AlGaAs and ρ is its resistivity. We measure a resistance between the gate and the 2DEG of 1.7×10^{11} Ω. We then estimate the resistivity to be $\rho = 1.6 \times 10^9$ Ω-m and calculate a dielectric relaxation time of 0.17 seconds at T = 10 K. This long relaxation time favors

the zero screening model for these 2 kHz measurements.

In summary, we conclude that while the deformation potential cannot account for the observed charge signal the piezoelectric effect can. If, however, we assume no screening, the predicted piezoelectric signal is a factor of three too large. Because the heterostructure used for the FET is composed of a well doped only on a single side, the 2DEG may reside near the gate side interface. While this structure lends itself to the extreme screening model, which predicts half the observed signal, the dielectric relaxation time doesn't favor screening at the 2 kHz measurement frequencies. Nonetheless, we speculate that the actual amount of screening that takes place may lie between these two extremes to account for the observed signal. It is difficult, however, to reach more definite conclusions using these simple models. I would like to note that the second model, the one involving the induced charge in the well and the two cladding interfaces, may still be valid for heterostructures having delta-doped layers on both sides of the well (see Figure 3.3b).

4.6 Strain Sensing at Higher Temperatures

In principle the strain sensing action of the FET will work at higher temperatures, even up to room temperature and above. We have not demonstrated room temperature operation due to constraints imposed by the low temperature design of the heterostructure material. For these heterostructures, higher temperatures result in a substantial decrease in the resistance between the gate and channel which causes the gate current to be larger than the drain current and renders the FET functionless. Although we have not demonstrated room temperature operation, we have repeated the 10 K measurements at 77 K and present the results below.

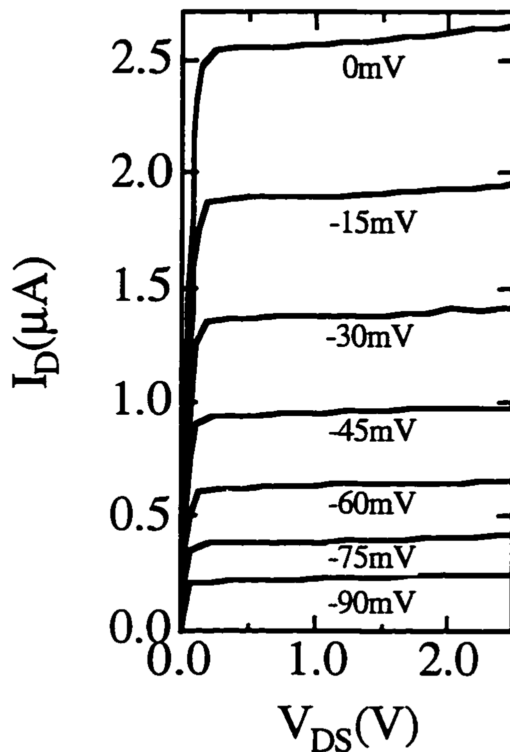


Figure 4.14 Drain characteristics at 77 K.

4.6.1 Strain Sensing at 77 K

For the 77 K measurements we used the same sample and experimental apparatus described above. We simply fill both inner and outer cans of the Infrared Labs Dewar with liquid nitrogen instead of liquid helium and perform the same set of measurements.

Figure 4.14 shows drain-source characteristics of the FET at T = 77 K. At a typical operating point, we measure a small signal drain-source resistance r_{ds} = 30 MΩ and a transconductance g_m = 30 μS which gives a transconductance per unit gate width of 6 mS/mm. Transconductance is a factor of 3 less than the 10 K value. A breakdown of the drain characteristics due to carrier heating was observed above V_{DS} = 3.5 V. For these voltages the electrons are given enough energy by the voltage drop along the channel to overcome the confining potential of the channel and diffuse either into the GaAs substrate or the gate.

Figure 4.15 shows a graph of normalized channel conductance as a function of gate voltage. Conductance changed by five orders of magnitude with V_{GS} from its zero gate voltage value G_o = 28 μS. The small magnitude of the pinch-off voltage (V_{po} = -130 mV) gives excellent sensitivity while the smooth, constant curvature indicates little parallel conduction.

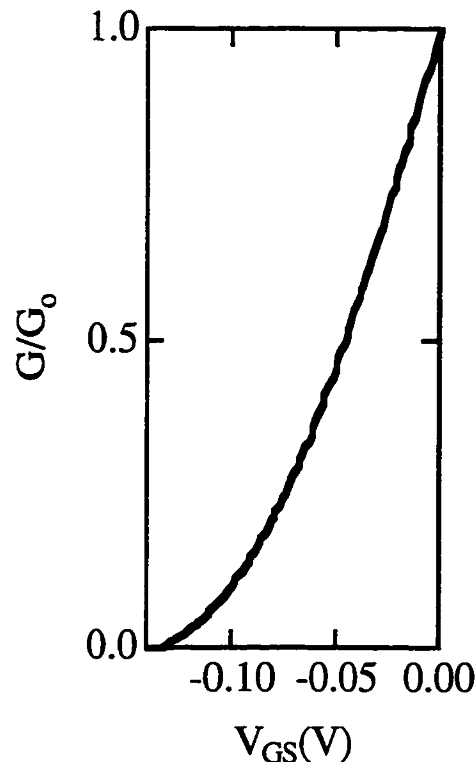


Figure 4.15 Pinch off graph of Channel conductance for the FET at 77 K

As with the FET described above, the measured gain and frequency response at 77 K agrees with simple field-effect transistor models. At a typical operating point, V_{GS} = -15 mV and I_D = 1.8 μA, the dimensionless voltage gain is A_v = 30. The gain was found to vary with a square root dependence on drain current: $A_v \propto I_D^{1/2}$ as expected. In our measurement, an RC rolloff occurred above a 3 dB point of 350 Hz due to Dewar lead capacitance ~ 450 pF. A figure of merit for the transistor speed, C_G/g_m where C_G is the capacitance between the gate and source, indicates an intrinsic rolloff frequency of 5 MHz.

Figure 4.16 shows a measured spectrum for voltage noise e_n referred to the input of the field-effect transistor for V_{GS} = -60 mV and I_D = 1.8 μA. The noise is characterized by a flat spectrum at high frequencies with a low 1/f noise corner ~ 1 kHz. In the saturation region the magnitude of the noise e_n is independent of drain-source voltage V_{DS} and drain

current I_D. The noise contribution from the external voltage sources and amplifiers is negligible. The white noise level corresponds to a gate charge noise $\delta q_g = e_n C_G < 0.7$ e/√Hz.

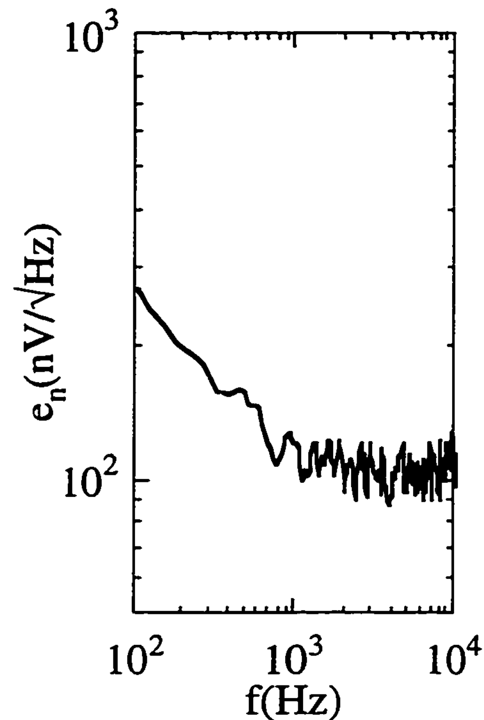


Figure 4.16 Noise spectrum for V_{GS} = -60 mV and I_D = -0.65 μA taken at T = 77 K and corrected for RC rolloff of the eternal circuit. The white noise level corresponds to a gate charge noise of 0.7 e/√Hz. The *1/f* noise corner is ~1 kHz.

A variable strain was applied to the field-effect transistor by using the bimorph to drive the chip through its lowest mechanical resonance. For the FET operating at V_{GS} = -15 mV and I_D = 1.8 μA, Figure 4.17 shows the FET small signal response v_{DS} measured as the chip is driven through its mechanical resonance. This voltage response is due mainly to the piezoelectric effect, which couples stress in the substrate to a change in electronic sheet density in the FET channel. At resonance, deflection was measured independently using a Michelson interferometer to obtain a volume strain in the region of the FET of 8 x 10^{-8}. The strain sensitivity at 77 K was found to be 4 x 10^{-9}/√Hz limited by FET noise. This value is a factor of two worse than the 10 K value indicating that the strain sensor's performance does not seriously degrade at 77 K.

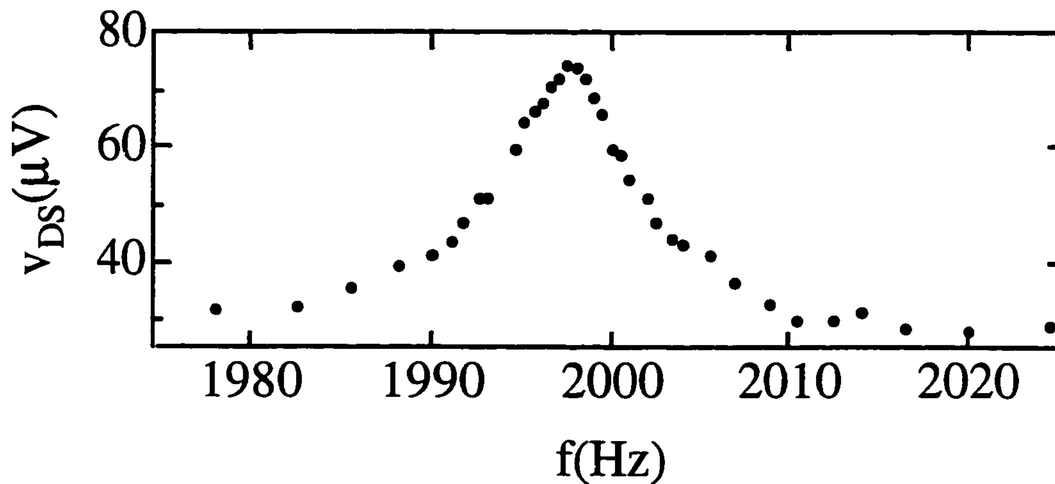


Figure 4.17 Small signal drain-source voltage v_{DS} for V_{GS} = -15 mV and I_D = 2 μA as FET substrate is driven through its lowest mechanical resonance.

One gains more intuition for the magnitude of this number by considering a cantilever with dimensions 100 μm x 20 μm x 1 μm with such a strain sensing FET integrated into its base. A strain sensitivity of 4×10^{-9} /√Hz will provide a force sensitivity of 32 pN/√Hz and a deflection sensitivity of 1 Å/√Hz at the free end of the cantilever. This performance prediction encouraged us to proceed to demonstrate strain sensing FETs as force or displacement sensors in scanning probe microscope cantilevers. This is the subject of the next chapter.

CHAPTER 5

SELF-SENSING CANTILEVERS

After we fabricated and characterized field-effect transistors and measured their strain sensitivity, we proceeded to fabricate freestanding cantilevers from GaAs/AlGaAs heterostructures containing a two-dimensional electron gas (2DEG). We integrate strain-sensing FETs into the cantilever base as force or displacement sensors. This chapter describes three heterostructure cantilevers each having an integrated strain-sensing field-effect transistor. Each of the three cantilevers represents an advance in the fabrication or operation of suspended structures containing a two-dimensional electron gas. Each also demonstrates a thinner device structure. The first device is a proof of principle self-sensing cantilever with dimensions 65 μm x 11.4 μm x 0.5 μm. This represented the first demonstration of a freestanding structure containing a two dimensional electron gas. The integrated transistor was used to measure the cantilever resonance frequency. The second cantilever has dimensions 65 μm x 11.4 μm x 0.25 μm and was used as a low temperature scanning probe microscope cantilever. The third cantilever with dimensions 3 μm x 2 μm x 0.129 μm represents a significant refinement in the fabrication of these

structures. The projected displacement sensitivity for this device is a factor of 5,000 greater than the larger lever and its FET characteristics may indicate lower noise behavior for thin suspended structures.

5.1 Measuring the mechanical resonance of a cantilever

Figure 5.1 shows the first cantilever we fabricated with a functional transistor at its base. The cantilever, with dimensions 65 μm x 11.4 μm x 0.5 μm, is fabricated from a $GaAs/Al_{0.3}Ga_{0.7}As$ heterostructure and contains a 2DEG. A strain sensing field-effect transistor integrated into the base acts as a low noise displacement sensor for the cantilever. The FET was used to measure the cantilever mechanical quality factor Q = 360 and resonance f_{res} = 88.2 kHz which is close to f_{res} = 91 kHz calculated from geometry. This cantilever demonstrated that it is possible to 1) fabricate free standing structures containing two dimensional electron gases and 2) make functional electronic devices on these structures that can be used to sense strain. The measurement of the mechanical resonance is an illustration of the higher frequency, dynamic operation of the FET as a strain sensor. Dynamic mechanical response points toward the operation of scanning probe microscope cantilevers in non-contact mode and also shows the ability of strain-sensing FETs to collect information on the mechanical response of small systems. This may have further application in the study of single dislocation motion or quantum effects, which can have a measurable effect on the mechanical response of a small beam operating at high frequencies.

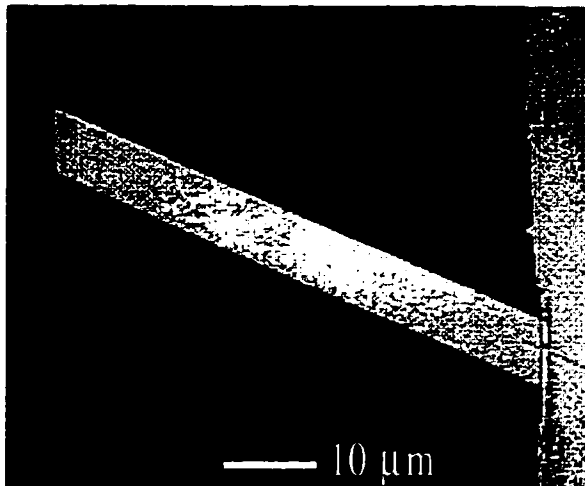


Figure 5. 1 Scanning electron microscope image of a GaAs/AlGaAs cantilever with an integrated strain-sensing field-effect transistor (FET). The FET gate can be seen at the cantilever base where the channel confines electrons to move on the suspended structure through the region of maximum strain. The alignment marker is on the substrate ~0.4 μm below the cantilever.

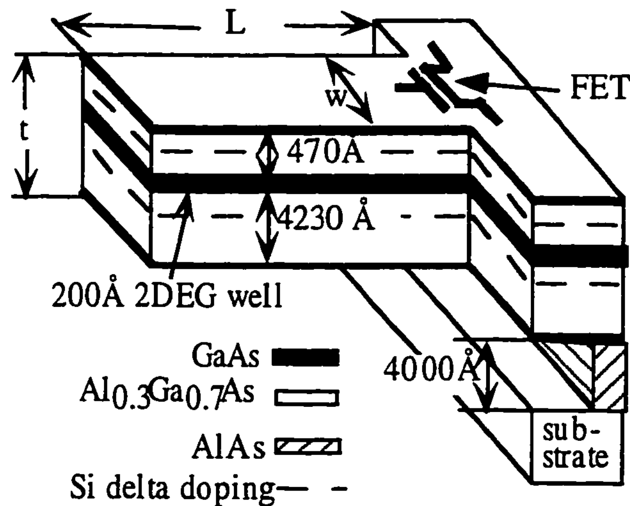


Figure 5. 2 Schematic showing the layer structure of the cantilever and wafer.

5.1.1 Integrated cantilever fabrication

In this section we describe the fabrication of the GaAs/$Al_{0.3}Ga_{0.7}As$ cantilever with an integrated strain-sensing FET shown in Figure 5.1. This structure was fabricated from a wafer containing a two-dimensional electron gas (2DEG) beginning 520 Å from the surface plus a 4000 Å sacrificial layer of AlAs beginning 5000 Å from the surface. The layers composing the cantilever shown in figure 5.2 in growth order are 100 Å GaAs, 4230 Å $Al_{0.3}Ga_{0.7}As$, 200 Å GaAs, 220 Å $Al_{0.3}Ga_{0.7}As$, Si delta doping layer at $8 \times 10^{12}/cm^2$, 250 Å $Al_{0.3}Ga_{0.7}As$ and 50 Å GaAs. The cantilever and FET were fabricated using four aligned electron-beam lithography steps. First, AuNiGe contacts were thermally evaporated through a resist mask composed of a bilayer of resist 3,100 Å thick with a lower layer of 4% 496 K molecular weight resist spun at 4,000 RPM and an upper layer of 2 % 950 K resist spun at 4,000 RPM. After the evaporation the resist was lifted off allowing the contacts to be thermally annealed to make ohmic contact to the 2DEG. Second, the FET channel was partially defined by etch trenches 750 Å deep formed by etching through a patterned resist mask 1,100 Å thick composed of 1 layer of 2% 950 K resist spun on at 4,000RPM. The etch was done using a 10:1 solution of 50% citric acid and 30% hydrogen peroxide. Third, the FET gate was formed by thermally evaporating 250 Å Cr and 2000 Å Au through a patterned mask followed by a standard liftoff technique. The resist mask had a thickness ~ 9,000 Å and was composed of a 4% 496 K resist spun at 4,000 RPM and a 6% 950 K resist layer spun at 6,000 RPM. The resulting gate to channel capacitance was calculated to be 9 fF based on geometry. The

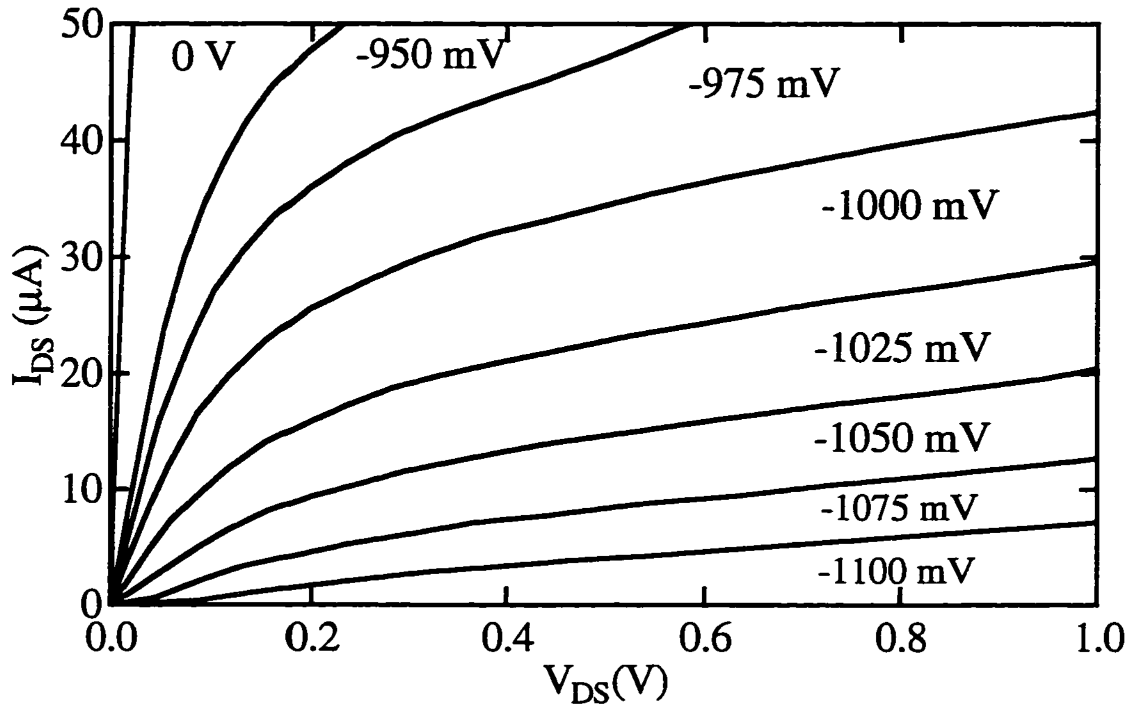


Figure 5. 3 Family of drain source curves I_{DS} vs. V_{DS} for the on cantilever FET taken at T = 4.2 K at the gate voltages indicated.

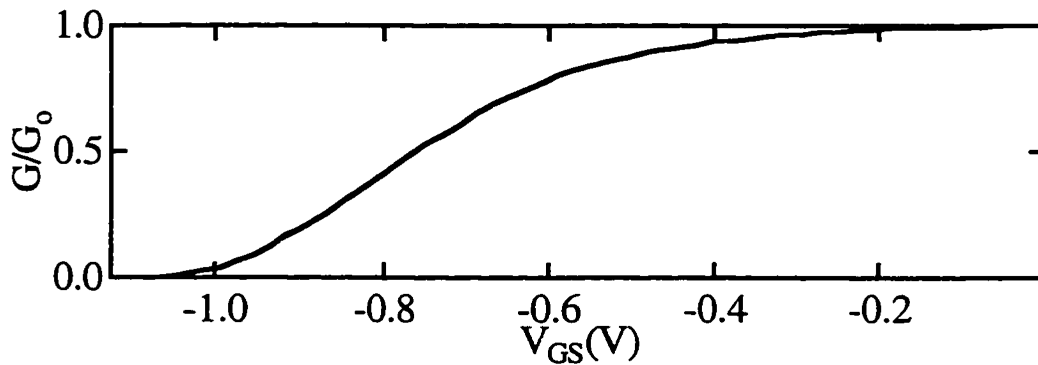


Figure 5. 4 Cutoff graph of channel conductance normalized to its zero gate voltage value of 2.5 mS. The cutoff voltage is V_c = -1.05 V.

fourth resist pattern laterally defined the cantilever to the desired dimensions of 11.4 μm wide by 65 μm long. With the cantilever and FET protected by a ~ 1 μm layer of resist composed of two layers of 6% 950 K resist spun at 6,000 RPM, a three minute reactive ion etch of 30 standard cm^3/min (sccm) BCl_3 and 20 sccm $SiCl_4$ at 50 mT pressure, 180

W power and -200 V dc bias was used to etch down and expose the underlying AlAs around the cantilever. The cantilever was then freed from the substrate by placing the sample in a 1:5 solution of 49% HF and water for about 15 seconds to selectively etch the underlying AlAs layer. The sample was then passivated by soaking it in a fluorinated thiol C-11 solution for two days as described in section 3.9. In order to prevent surface tension from either breaking the cantilever or causing it to stick to the substrate a CO_2 critical point dryer was used to remove the sample from the liquid into the air.

5.1.2 On-cantilever transistor characteristics

The channel of the field-effect transistor was 5.8 μm wide by 0.7 μm long and was integrated into the base of the cantilever. Figure 5.2 shows the drain source characteristics I_{DS} vs. V_{DS} of the on-cantilever FET for the series of gate voltages V_{GS} indicated. We measure a small signal transconductance $g_m = 0.3$ mS and drain-source resistance $r_{DS} = 16$ kΩ for a drain current of 73 μA. Figure 5.3 shows channel conductance normalized to its zero gate voltage value of 2.5 mS as the gate voltage V_{GS} is made more negative. The cutoff voltage $V_{GS} = -1.05$V is the voltage for which the channel conductance has decreased by a factor of 100. The FET noise power has a 1/f spectrum at low frequencies. At 90 kHz, the frequency of interest for this experiment, we measured a voltage noise $\delta v_g \sim 450$ nV/√Hz corresponding to a nominal gate charge noise $\delta q_g < 0.1$ e/√Hz. The frequency response of the FET shows that transconductance is constant up to the measured frequency of 100 kHz. The calculated time constant for

the FET gives a cutoff frequency [Sze, (1981)] $g_m/2\pi C_G \sim 5.3$ GHz where C_G is the gate to channel capacitance.

5.1.3 Measuring the mechanical resonance

The FET characterization measurements and the following cantilever measurements were taken at T = 4.2 K with the sample mounted in vacuum in an Infrared Labs Dewar. In order to excite the cantilever through its resonance frequency, we use the same experimental setup used to measure the strain sensitivity of the FET shown in figure 4.1(b). The sample was attached to a rigid Macor block that in turn was mounted to a piezoelectric bimorph. The sample was electrically shielded from the bimorph voltages by means of a grounded mount and protected from unwanted deformation by the rigid block. For the measurements below, the FET was biased with V_{GS} = -1.0 V and V_{DS} = 0.20 V resulting in a power dissipation of 4.4 μW. A constant drain-source voltage was applied using low noise battery-powered voltage sources while the drain current was monitored with an Ithaco 1211 current amplifier. Measuring the current using the Ithaco 1211 has the advantages of reducing the effect of Dewar lead capacitance and increasing the bandwidth of the signal from the Dewar; the Ithaco current amplifier places the source at a virtual ground thus eliminating the need to charge the source lead-ground capacitor. In this configuration, one doesn't observe the low RC rolloff ~400 Hz observed when measuring a voltage from the drain side of the FET. The dominant RC rolloff is given by the Ithaco amplifier itself where a ~1 pF feedback capacitance must be charged by the gain dependent current amplifier resistor. A Stanford Research 530 digital

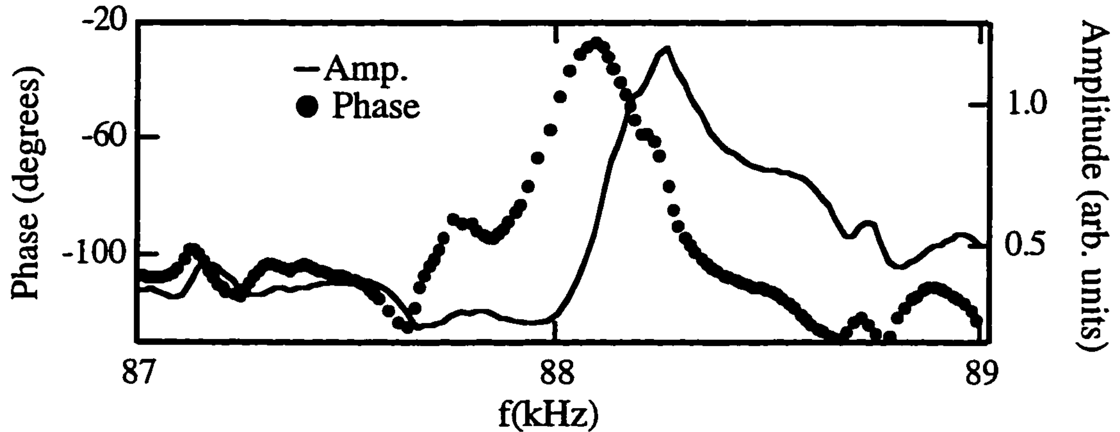


Figure 5. 5 Measured FET response as the cantilever is driven through its mechanical resonance. Both amplitude (solid line) and phase with respect to the piezoelectric driving voltage (dots) were recorded.

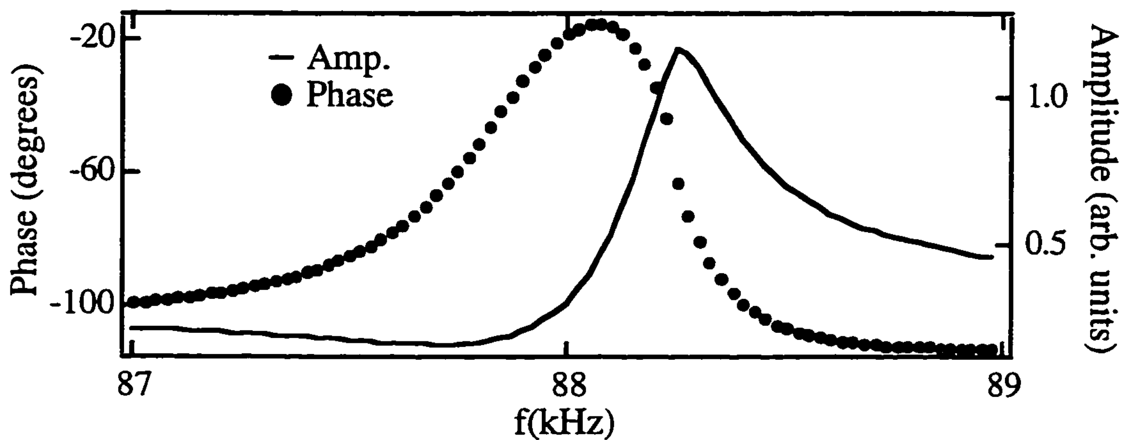


Figure 5. 6 Results of a model calculation explaining the shapes of the measured curve by including the cantilever resonance signal and the effect of the capacitive coupling between the bimorph driving circuit and the measurement circuit.

lock-in amplifier referenced to the bimorph-driving signal was used to monitor the output of the Ithaco 1211. As the cantilever was driven through its mechanical resonance, both drain current amplitude and phase with respect to the bimorph driving voltage were measured.

Figure 5.5 shows a graph of FET drain current amplitude and phase with respect to the driving voltage as the cantilever is driven by the piezoelectric bimorph. The peaks in amplitude and phase indicate that the cantilever is passing through its mechanical resonance. Through resonance, one would expect a peak in amplitude and a phase shift of $-\pi$ radians. We observe a peak in amplitude and phase. The shapes of these curves can be understood by a model involving the strain-induced FET signal added to a constant term due to capacitive coupling between the bimorph driving circuit and the measurement circuit. If one adds these phasors together a result with a similar shape to the data will be found. Figure 5.6 shows results of a model calculation where the measured signal amplitude A_S and phase ϕ_S are modeled by:

$$A_s exp(i\phi_s) = exp(i\phi_{amp})\{A_C\, exp(i\pi/2) + A_{res}(f) exp[i\phi_{bim} + i\phi_{res}(f)]\} \qquad (5.1)$$

where ϕ_{amp} is the phase shift due to the external amplifier, $A_C\, exp(i\pi/2)$ is the capacitive term, ϕ_{bim} is the phase shift between bimorph and cantilever excitation due to driving the bimorph above its resonance frequency of 400 Hz, and

$$A_{res}(f) = \frac{\beta}{\sqrt{(f_{res} - f)^2 + \gamma^2/4}} \text{ and } \phi_{res}(f) = \tan^{-1}\left(-\frac{\gamma}{2(f_{res} - f)}\right)$$

are the frequency dependent amplitude and phase of the cantilever where f_{res} is the resonance frequency and β and γ are parameters whose values are estimated from the measured resonance curves. Parameters for (5.1) were chosen in the following way. For frequencies off resonance $A_{res}(f)$ becomes negligible and the signal had a measured amplitude of 0.3 and phase of $-120°$ which gives a value for A_c and ϕ_{amp} of 0.3 and 150°

respectively. Values for β and γ are chosen by measuring the height and width of the resonance and ϕ_{bim} is a free parameter found to be about 310°. Figure 5.6 shows that this equation produces a shape very similar to the data. Measurements indicate a mechanical quality factor Q = 360 and resonance frequency f_{res} = 88.2 kHz which is lower than the theoretically predicted value of 91 kHz obtained from cantilever geometry. This measurement demonstrates that strain-sensing FETs can be used to dynamically monitor the mechanical response of a GaAs/AlGaAs cantilever.

5.2 Scanning Probe Microscope Cantilevers

The above cantilever demonstrated a 0.5 μm thick, freestanding structure containing a two-dimensional electron gas. We now demonstrate a thinner, 0.25 μm, cantilever that will be used as a scanning probe microscope cantilever in a low temperature scanning probe microscope built by Mark Eriksson. A complete description of the microscope can be found in Mark's doctoral thesis [Eriksson, (1997)].

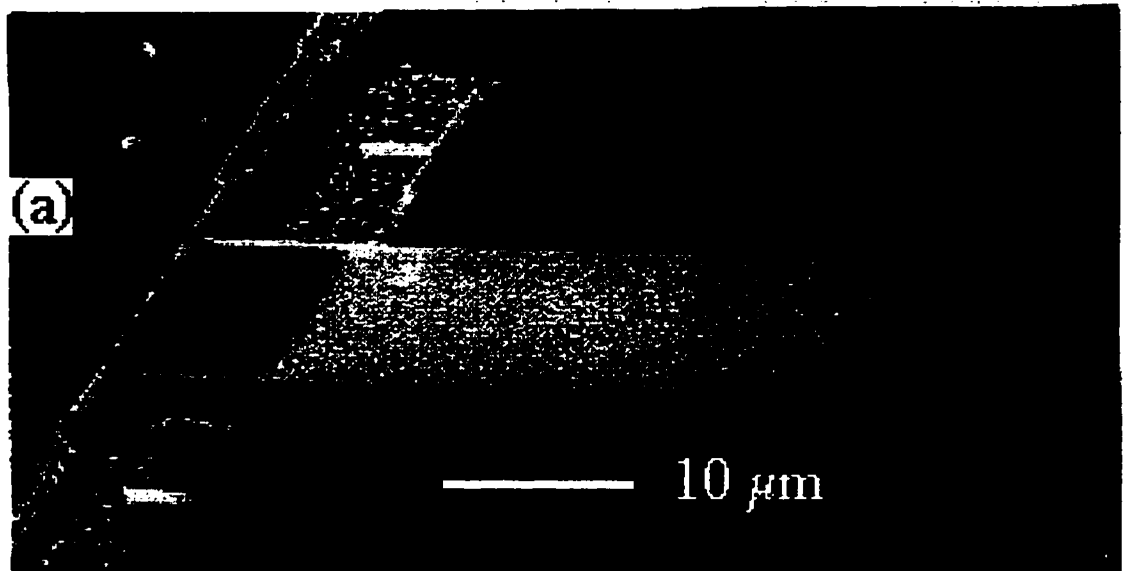
5.2.1 Introduction to self-sensing cantilevers

The invention of the atomic force microscope [Binnig et al. (1986)] has profoundly impacted surface imaging and has spurred the exploration of new types of scanning probe microscopy (SPM). The deflection of scanning probe cantilevers has been detected by using tunneling current [Binnig et al. (1986)], optical levers and interferometers [Rugar et al. (1988)], capacitance [Brugger et al. (1994)], piezoresistance [Tortonese et al. (1992)], and piezoelectrics [Watanabe et al. (1996); Itoh et al. (1994); Tansock et al. (1992)]. Recently, strain sensors have been demonstrated comprised of field-effect transistors (FETs) fabricated from a GaAs/AlGaAs heterostructure containing a two-dimensional electron gas (2DEG) [Beck et al. (1996); Fung et al. (1997)]. Such

strain sensors can be used in heterostructure SPM cantilevers and also have broader potential applications for detecting forces and displacements in GaAs/AlGaAs micro-electromechanical systems (MEMS) [Cleland et al. (1996); Tighe et al. (1997)].

In this section we describe the fabrication and operation of a GaAs/$Al_{0.3}Ga_{0.7}As$ SPM cantilever with an integrated strain-sensing FET at its base. Strain-sensing FETs offer advantages for cantilever deflection sensing. Because the strain sensor is integrated into the cantilever, no external deflection sensors are needed, and micron scale cantilevers and more complex micro-electromechanical systems become feasible. Both the force and displacement sensitivities of strain-sensing cantilevers improve with scaling to smaller sizes, and the resonant frequency increases. The strain sensing FET provides gain, reducing the cantilever power dissipation by several orders of magnitude compared with piezoresistive strain sensors. Small size, high operating frequency, and low power dissipation make strain-sensing FETs ideal for use in small cantilevers [Walters et al. (1996)] and other MEMS.

We describe here a proof of principle device, which demonstrates the integration of strain-sensing FETs into SPM cantilevers. The FET has a gate 5 μm wide by 0.75 μm long with a measured small-signal transconductance $g_m = 0.3$ mS and drain-source resistance $r_{ds} = 50$ kΩ at drain current $I_{DS} = 50$ μA. The noise has a 1/f spectrum between 10 Hz and 1 kHz with $\delta v_g = 1$ μV/√Hz at 100 Hz corresponding to a charge noise $\delta q_g \sim 0.1$ e/√Hz, where δv_g and δq_g are the gate voltage and charge noise. The FET is fabricated at the base of a cantilever with dimensions 65 μm x 11.4 μm x 0.25 μm and a calculated spring constant 19 mN/m and resonant frequency 46 kHz. A tip is formed by defining the cantilever into the shape of a point. The vertical resolution was measured to be 10 Å/√Hz at 100 Hz corresponding to a force resolution of 19 pN/√Hz, limited by FET noise. We imaged a mica grating at T = 2.2 K.



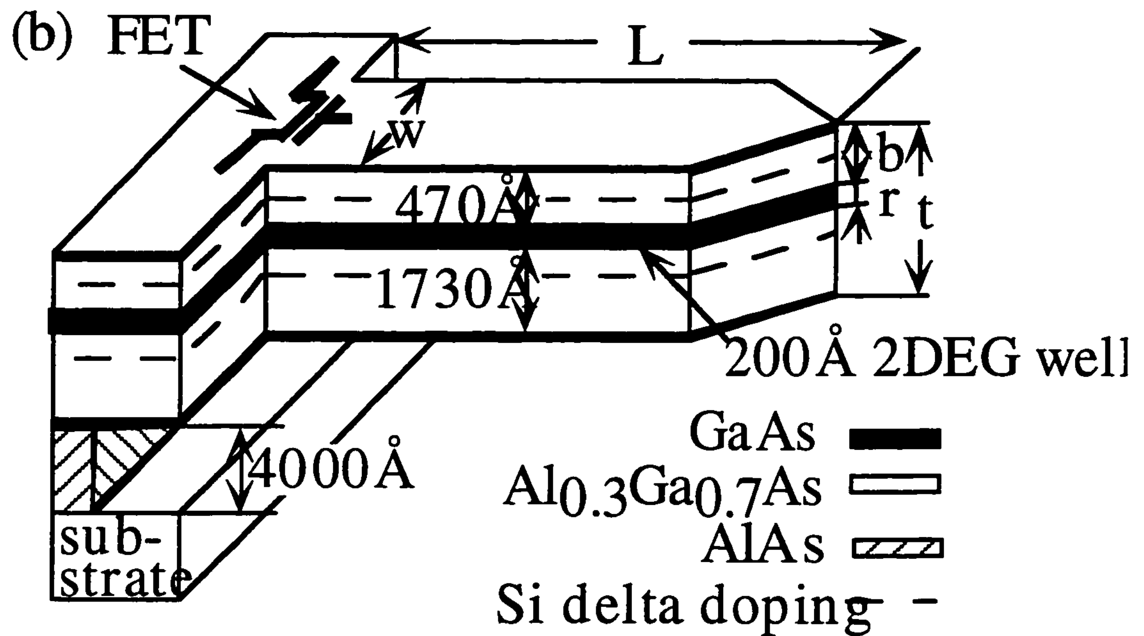


Figure 5. 7 (a) SEM image showing a GaAs/AlGaAs cantilever, 11.4 μm x 65 μm x 0.25 μm, with a strain sensing field-effect transistor (FET) at its base. The cantilever is lithographically defined into the shape of a point to act as a tip. Both the FET gate and an etch trench can be seen at the cantilever base showing that electrons flow through the region of maximum strain on the suspended structure of the cantilever itself. (b) Schematic of the epitaxial layer structure of the wafer and cantilever.

5.2.2 Scanning probe microscope cantilever fabrication

Figure 5.7(a) shows an SEM image of a cantilever with a strain-sensing FET at its base. Figure 5.7(b) is a schematic of the epitaxial layers of the wafer and cantilever. The layers composing the cantilever in growth order are100 Å GaAs, 1510 Å $Al_{0.3}Ga_{0.7}As$, Si delta doping layer at 2 x 10^{12} /cm^2, 220 Å $Al_{0.3}Ga_{0.7}As$, 200 Å GaAs, 220 Å $Al_{0.3}Ga_{0.7}As$, Si delta doping layer at 8 x 10^{12} /cm^2, 250 Å $Al_{0.3}Ga_{0.7}As$ and 50 Å GaAs. The FET and cantilever were fabricated using four aligned electron-beam lithography steps in a manner similar to the fabrication procedure described above. All resist layers are the same as described in section 5.1.1 and will be omitted here. First, AuNiGe contacts were deposited by thermal evaporation through a patterned resist and annealed to make ohmic contacts to the 2DEG. Second, an etch trench, visible at the left side of Figure 5.7a, was patterned that confined electrons to flow onto the cantilever. This 750 Å deep trench was etched by a 10:1 solution of 50% citric acid and 30% hydrogen peroxide at T = 50° C. Third, the FET gate with dimensions 5 μm x 0.75 μm composed of 200 Å Cr and 2500 Å Au and having a nominal gate to channel capacitance of 8 fF was patterned using lift-off techniques. Fourth, the lateral pattern of the cantilever with a pointed tip and dimensions 11.4 μm wide and 65 μm long was lithographically defined. A vertical trench around the cantilever was cut using a 3 minute reactive ion etch of 30 sccm BCl_3 and 20 sccm $SiCl_4$ at 50 mT pressure, 180 W power and -200 V dc bias to expose the underlying sacrificial layer of AlAs. The AlAs layer was selectively etched to free the cantilever from the substrate by using a 1:5 solution of 49% HF:H_2O. The sample was soaked in a C-11 fluorinated thiol solution for two days in order to coat the structure with a self-assembled monolayer. To prevent the cantilever from either breaking or sticking to the substrate due to surface tension, a CO_2 critical point dryer was used to remove the free cantilever from liquid to air. The substrate beneath the cantilever

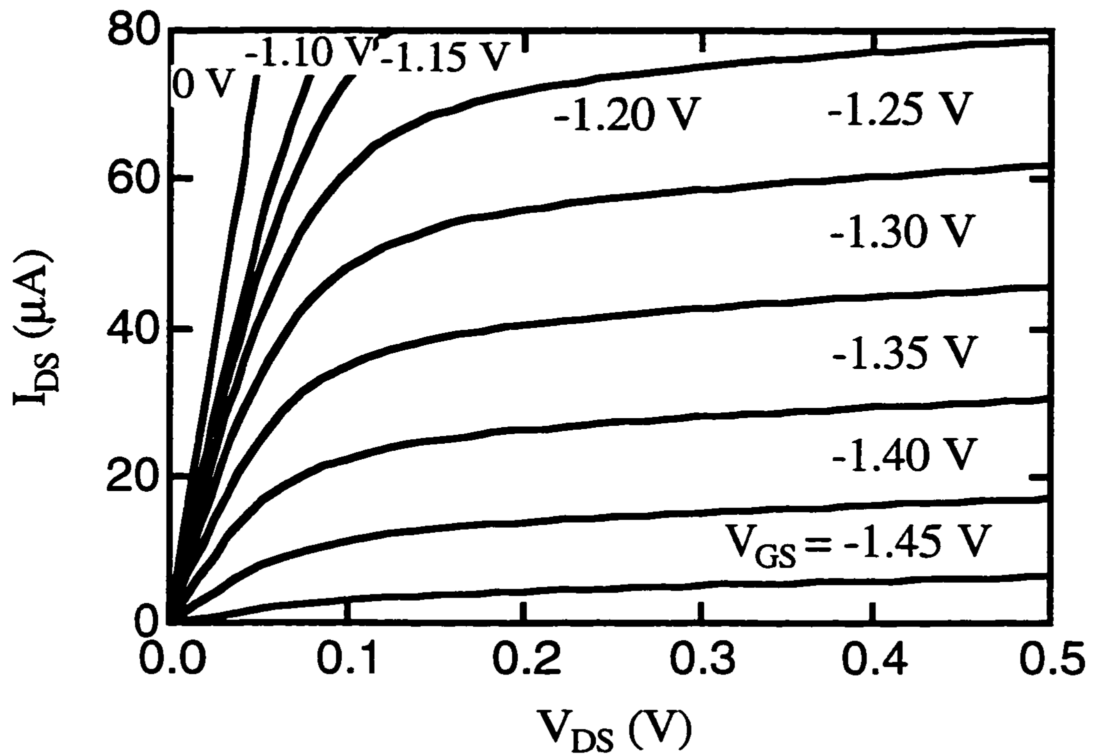


Figure 5. 8 Family of source-drain characteristics for the on-cantilever FET taken at T = 4.2 K for the gate-source voltages indicated.

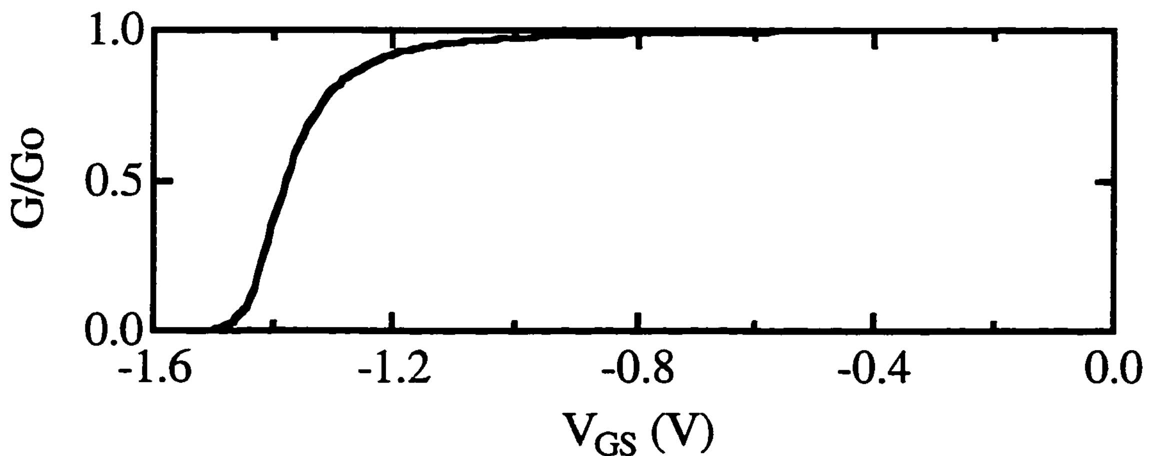


Figure 5. 9 Cutoff graph of channel conductance normalized to its zero gate voltage value of 0.27 mS. The cutoff voltage is V_{gs} = -1.5 V.

was cleaved away using the jig described in section 3.2 allowing the cantilever to contact a sample for imaging.

5.2.3 On-cantilever transistor characteristics

Figure 5.8 shows drain-source characteristics I_{DS} vs. V_{DS} for the on-cantilever FET at a series of gate voltages at temperature T = 4.2 K. The small signal transconductance is $g_m \cong 0.3$ mS and drain source resistance is $r_{ds} \cong 50$ kΩ at $I_{DS} = 50$ μA. Figure 5.9 shows the cutoff in channel conductance G with V_{GS} normalized to its zero gate voltage value of $G_o = 0.27$ mS. The cutoff voltage $V_{GS} = -1.5$ V for channel conductance was determined from an expanded plot of Fig. 5.9. The frequency response for a nominally identical FET was flat up to the measurement limit of 100 kHz, and the cutoff frequency inferred from the RC time of the transistor is $g_m/2\pi C_G = 6$ GHz.

5.2.4 Scanning probe cantilever performance

The cantilever was mounted in vacuum as part of a low temperature scanning probe microscope [Eriksson, (1997)]. The cantilever deflection was monitored by dc voltage biasing the FET channel and gate while monitoring the drain current with an Ithaco 1211 current amplifier. The bias point used for the measurements below was $V_{GS} = -1.30$ V and $V_{DS} = 0.30$ V resulting in a power dissipation of 7.2 μW. Care was taken to shield the cantilever from the high voltages required to operate the SPM scanning tube. A mica sin(x)sin(y) grating with 1 μm period and 200 nm peak-to-peak amplitude was used to test the imaging capability of the cantilever. Measurements were taken at 4.2 K and 2.2 K.

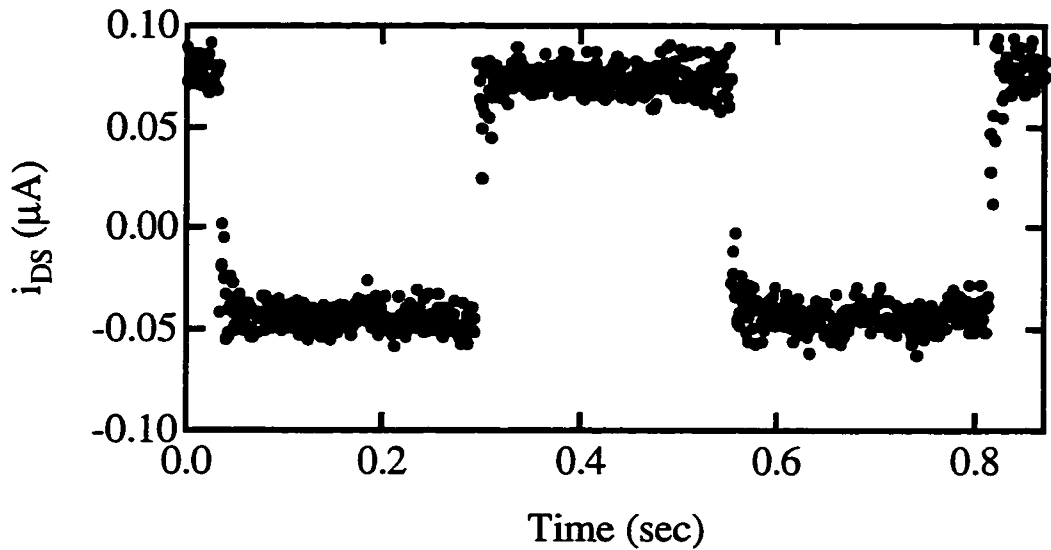


Figure 5. 10 FET response as cantilever is deflected at a frequency of 2 Hz by a step deflection of amplitude 0.4 μm corresponding to a step force of 7.6 nN.

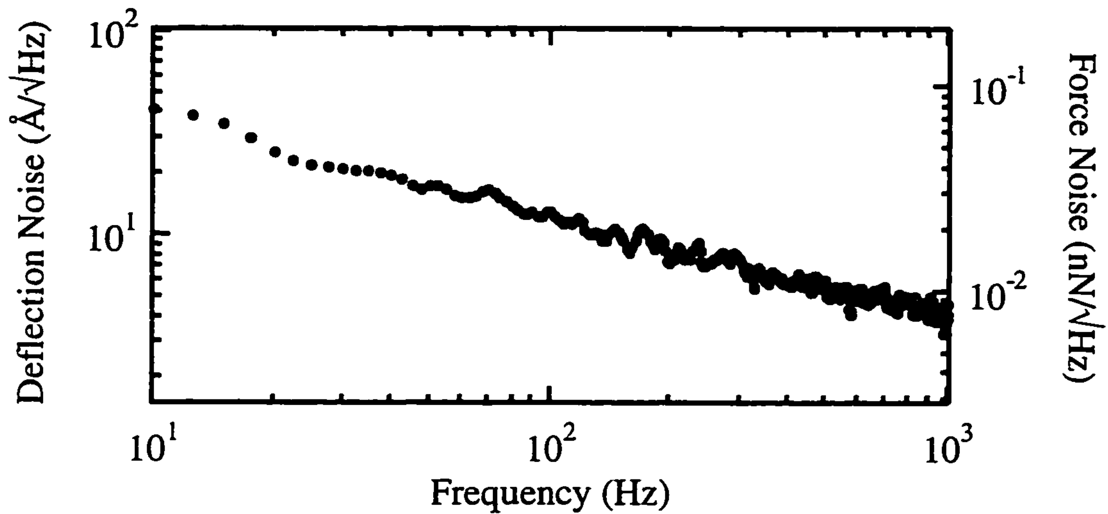


Figure 5. 11 Measured noise spectra of FET on a freestanding cantilever converted to units of deflection and force noise.

Figure 5.10 shows the current response of the FET for a square wave deflection of the tip with frequency 2 Hz and peak-to-peak amplitude 0.4 μm, corresponding to a tip force 7.6 nN. Figure 5.11 shows a graph of cantilever deflection noise and force noise measured for a freestanding cantilever. The noise power referred to input has a 1/f

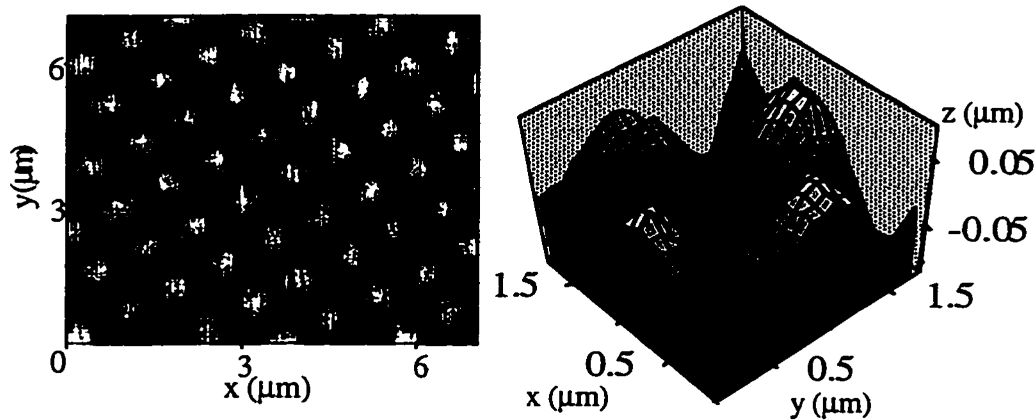


Figure 5.12 Left: 7 μm x 7 μm image taken using the strain-sensing cantilever. Structure is a sin(x)sin(y) mica grating with spacing 1 μm and depth 200 nm. Figure 5.13 Right: A smaller scan demonstrating the finer vertical resolution of the cantilever.

spectrum in the frequency range between 10 Hz and 1 kHz and was found to be independent of gate voltage and drain-source voltage in the operating region of the FET. The measured deflection sensitivity is limited by FET noise; mechanical thermal noise and amplifier noise are negligible at these frequencies. Empirically, the 1/f noise current is found to be proportional to $1/\sqrt{N}$[Weissmann, (1988); Duh et al. (1983)] here N is the number of switching sites. Thus, 1/f noise current $\propto 1/\sqrt{\text{(gate area)}}$ and could be reduced by a factor ~ 10 by increasing the area of the FET gate to cover more of the strained region at the cantilever base.

Figure 5.12 presents a 7 μm x7 μm SPM image of a mica calibration grating with period 1 μm and peak-to-peak amplitude 200 nm taken using the strain-sensing cantilever at T = 2.2 K. The tip deflection was recorded in a 1 kHz bandwidth as the tip was scanned across the grating. Figure 5.13 with a smaller scan range demonstrates the finer vertical resolution of the cantilever.

5.2.5 Comparison of cantilever response with theory

Strain-sensing FETs operate via the piezoelectric effect. Deflection of the cantilever produces a strain field $\varepsilon(x) = 2\varepsilon_0 x/t$ in the plane of deflection, where x is the distance from the center of the cantilever along the growth direction, and ε_0 is the maximum strain at the cantilever surface (the elastic moduli of GaAs and $Al_{0.3}Ga_{0.7}As$ differ by 0.6%). The strain produces polarization in the form of volume bound charge throughout the cantilever as well as sheets of bound charge at every interface. We assume the free electrons in the channel screen the bound charge induced in the region occupied by the 2DEG producing an effective gate charge ΔQ. Because this measurement is taken at 2 Hz, we assume screening of polarization outside of the well. For this heterostructure, with doping on both sides of the quantum well as seen in Figure 3.2, we model the change in charge in the 2DEG to be equal to the charge induced in the well and its two cladding interfaces. Thus, following equation 4.21, the change in FET current ΔI for tip deflection Δz due to the charge induced in the quantum well and the two cladding interfaces is

$$\Delta I = \frac{g_m \Delta Q(\Delta z)}{C_G} \cong \frac{3 E g_m b r d_{12AlGaAs}}{\varepsilon L^2} \Delta z \qquad (5.2)$$

where C_G is the gate-to-channel capacitance, E is Young's modulus, $d_{12AlGaAs}$ is the row 1 column 2 component of the piezoelectric tensor for $Al_{0.3}Ga_{0.7}As$, ε is the dielectric constant for $Al_{0.3}Ga_{0.7}As$ and the dimensions L, r, and b are indicated in Figure 5.7(b). The measured signal ΔI in Fig. 5.9 agrees with Equation (5.2) to within 20%. This model assumes that polarization outside the region occupied by the 2DEG is screened and doesn't contribute to the signal. Including the effect of the polarization induced outside the well increases the calculated signal by a factor of three. While most piezoelectric cantilevers are limited to dynamic operation faster than the dielectric relaxation time,

strain-sensing FETs retain their function for static deflections, because the screening electrons in the 2DEG provide the signal.

5.2.6 Advantages of integrated strain-sensing cantilevers

While the system demonstrated here is a proof of principle, the advantage of strain-sensing FETs over other types of displacement sensors is manifested in how performance parameters scale to small sizes. First, strain-sensing cantilevers gain sensitivity as their size is reduced. This can be seen by considering an FET with a minimum detectable strain ε_{min} at the cantilever surface. Both the minimum detectable force

$$F_{\min} = (\frac{Ewt^2}{6L})\varepsilon_{\min} \quad (5.3)$$

and displacement

$$U_{\min} = (\frac{2L^2}{3t})\varepsilon_{\min} \quad (5.4)$$

decrease as the cantilever is scaled to smaller sizes keeping the same aspect ratios. Here E is Young's modulus for the cantilever and the dimensions are defined in Figure 5.7(b). Second, smaller cantilevers have higher resonant frequencies and lower power dissipation. At frequencies above the 1/f noise corner, piezoresistive strain sensors are ultimately limited by Johnson noise and have a signal to noise ratio (SNR) of

$$(SNR)^2 = \left(\frac{\Delta V}{\delta v_J}\right)^2 = \frac{I^2 \Delta R^2}{4k_B T R \Delta f} = \left(\frac{\Delta R}{R}\right)^2 \frac{P_B}{4k_B T \Delta f} \quad (5.5)$$

where ΔV is the voltage signal, ∂v_J is the rms Johnson noise magnitude, ΔR is the change in resistance R, I is the resistor current, P_B is the power dissipation associated with the readout current, k_B is Boltzmann's constant, T is the sample temperature and Δf is the measurement bandwidth. For two-dimensional resistors, R, SNR , and the power P_B (~1 mW) required to maintain a good SNR are independent of size scale. Thermal conductance of this heat away from small cantilevers will ultimately limit how small they can be. In contrast, strain sensing FETs provide large power gain thus lowering the power required for good sensitivity to small values (~10 μW) and permitting operation at small size scales. For FETs operating above the $1/f$ noise corner the noise figure NF_o defined in section 2.3.2 for a given frequency f is dominated by the gate metallization resistance r_m and the source access resistance r_s and is empirically found to be [Fukui et al. (1978)]

$$NF_o \cong 1 + 0.25L_c f[g_m(r_s + r_m)]^{1/2} \qquad (5.6)$$

where L_c is the gate length. For small sizes the projected noise figure NF_o improves. Thus, the scaling characteristics of strain-sensing FETs show promise for sensitive high speed imaging applications [Walters et al. (1996)].

5.3 Smaller cantilevers

The advantage of using strain sensing field-effect transistors for scanning probe microscopes can be realized as the cantilever is made smaller in size. As seen in equation (5.3) and (5.4), both force and displacement sensitivities improve for small sizes, and resonant frequency

$$f_{res} = 0.16\sqrt{\frac{E}{\rho}}\frac{t}{L^2} \qquad (5.7)$$

increases. We have fabricated a cantilever with dimensions 3 μm x 2 μm x 0.129 μm that is projected to have a 5000-fold improvement in deflection sensitivity and a 19-fold improvement in force sensitivity over the sensitivities described above, and a resonant frequency of 11 MHz. This cantilever has the potential to sensitively scan at high speeds.

5.3.1 Small cantilever fabrication process

Figure 5.14a shows an image of a small cantilever with dimensions 3 μm x 2 μm x 0.129 μm with an integrated FET and a carbon tip grown by electron beam deposition. A second FET visible in Figure 5.14b is fabricated behind the cantilever to enable differential measurements. The layer structure of the cantilever is similar to that shown in figure 5.7(b) except for a thinner AlGaAs layer on the substrate side of the quantum well. In growth order along the [100] crystal direction, the layers are 100 Å GaAs, 250 Å $Al_{0.3}Ga_{0.7}As$, Si delta doping layer at 5×10^{12} /cm^2, 220 Å $Al_{0.3}Ga_{0.7}As$, 200 Å GaAs, 220 Å $Al_{0.3}Ga_{0.7}As$, Si delta doping layer at 8×10^{12} /cm^2, 250 Å $Al_{0.3}Ga_{0.7}As$ and 50 Å GaAs giving a total cantilever thickness of 1290 Å. From this wafer we cleave a rectangular chip with edges along the 011 and $0\bar{1}1$ directions. Two additional cleaves, one along the $10\bar{1}$ plane and another along the $1\bar{1}0$ plane, cut off the corners of the chip making one side of the once rectangular chip a point and leaving an undercut profile (see Figure 3.4(b)). Fabrication is performed such that the cantilever is along the $0\bar{1}1$ direction for the maximum strain effect and ~50 μm from the point as seen in Figure 5.14c to facilitate contact to a sample with this short, 3 μm lever.

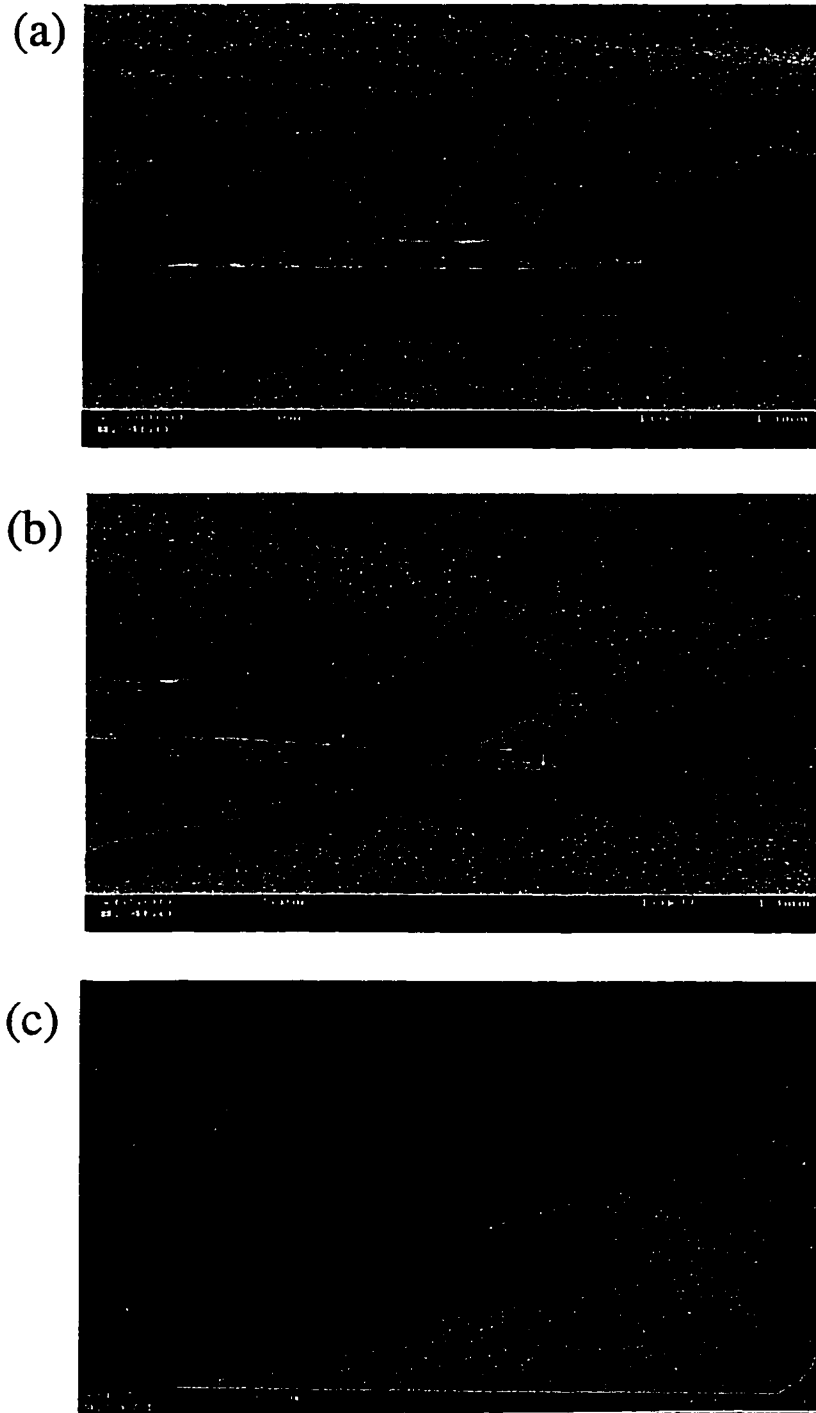


Figure 5.14 (a) SEM micrograph of a self-sensing cantilever 3 μm x 2 μm x 0.129 μm with an integrated strain-sensing FET and an electron beam deposited tip. The thicker gate lead can be seen behind the cantilever. (b) Larger view showing the reference FET (c) Larger view showing the cantilever and the edge of the chip. Fabrication took place ~ 50 μm from the chip's edge.

Six electron beam lithography steps are required for cantilever fabrication. For each step, resist is applied using the off-axis spinner chuck shown in Figure 3.6, with the point of the chip pointing toward the center of the spinner chuck to eliminate the unwanted resist bead close to the fabrication region. First, AuNiGe contacts that enable a two-probe measurement of each FET channel are deposited through a resist mask composed of 2 lower layers of 4 % 496 K resist spun at 500 RPM and 2 upper layers of 6% 950 K resist spun at 500 RPM, lift off is performed and the contacts are thermally annealed. Second, etch trenches are patterned, using a resist of 2 layers of 6 % 950 K spun at 400 RPM, to confine electrons to the channels of the FETs and remove the 2DEG from beneath what will be the FET gate and gate leads. Trenches, 650 Å deep, are made by ion milling for 85 seconds through the ~0.5 μm thick layer of resist using the parameters of beam current 23 mA, beam voltage 500 V, accelerator voltage 300 V and argon pressure of 2 mT. Third, the gates, gate leads, and contacts are defined using a resist of 2 layers 4 % 496 K spun at 400 RPM followed by one layer 6 % 950 K spun at 500 RPM. A thin film of 50 Å Cr and 150 Å Au is thermally deposited, and liftoff is performed. Fourth, using the same resist structure as for AuNiGe contacts, the entire gate structure is repatterned with the exception of what will be the on-cantilever gate, and a thick layer of metal, 200 Å Cr and 1000 Å Au is thermally deposited and lifted off. The two gate metal evaporation steps produce a thin gate over the cantilever to reduce gate effects on mechanical response and thick gate leads and contacts to reduce gate metallization resistance and hence Johnson noise. These two gate layer thicknesses can be seen in Figure 5.14(b). Fifth, the lateral dimensions of the cantilever are patterned through a thick ~ 1μm resist (4 layers of 6 % 950 K spun at 500 RPM) and the ion miller is used with the same parameters as above for 4 minutes to etch down and expose the underlying AlAs layer.

The resist is removed and the chip is coated with paraffin by dipping it in a Xylene/paraffin solution described in section 3.11 and drying it in air under a 100 Watt

light bulb. The chip is placed in the SEM where a carbon tip is grown by placing the electron beam on the end of the cantilever for 105 sec with beam parameters, 15 keV, 3.0 pA, mag 40000, and working distance 8 mm. Residual paraffin was removed in Hexanes and ultrasound and the chip was further cleaned using an oxygen reactive ion etch for ~ 3 min with pressure 70 mT, power 10 W, DC bias –250 V and O_2 flow 50 sccm. Finally, the chip was dipped in a 1:15 solution of HF:H_2O for 5 seconds and soaked in a C-11 fluorinated thiol solution for 2 days to allow a self-assembled monolayer to coat the entire sample. Because of the cantilever's small size, critical point drying is not necessary, hence the cantilever was taken out of ethanol and allowed to dry on a piece of filter paper. It was now ready for wirebonding and mounting in the Dewar.

5.3.2 On-cantilever FET characteristics

This fabrication procedure produced an on-cantilever field-effect transistor with channel width 1 μm and length 8 μm having a nominal gate/channel capacitance of 16 fF. The transistor exhibits a typical small-signal drain-source resistance 4 MΩ and transconductance 30 μS for a drain current I_D = 10 μA and drain-source voltage V_{DS} = 0.75 V giving a transconductance per unit gate width of 30 mS/mm. The noise power is characterized by a *1/f* spectrum at low frequencies having a voltage noise value of $\delta v_g \sim$ 10 nV/√Hz at 2 kHz where it runs into the noise floor of the Ithaco amplifier. The corresponding gate charge noise at 2 kHz is $\delta q_g \sim 0.001$ e/√Hz. This provides a low noise strain sensor for cantilever deflection sensing. The reference FET had similar channel dimensions, exhibited a small signal drain source resistance 4 MΩ and a transconductance of 25 μS at I_D = 8.1 μA and V_{GS} = 0.75 V. Its noise power has a *1/f* spectrum over the frequencies of interest and was approximately 10 times larger than the cantilever FET noise magnitude. This may be due to its close proximity to the exposed AlAs layer.

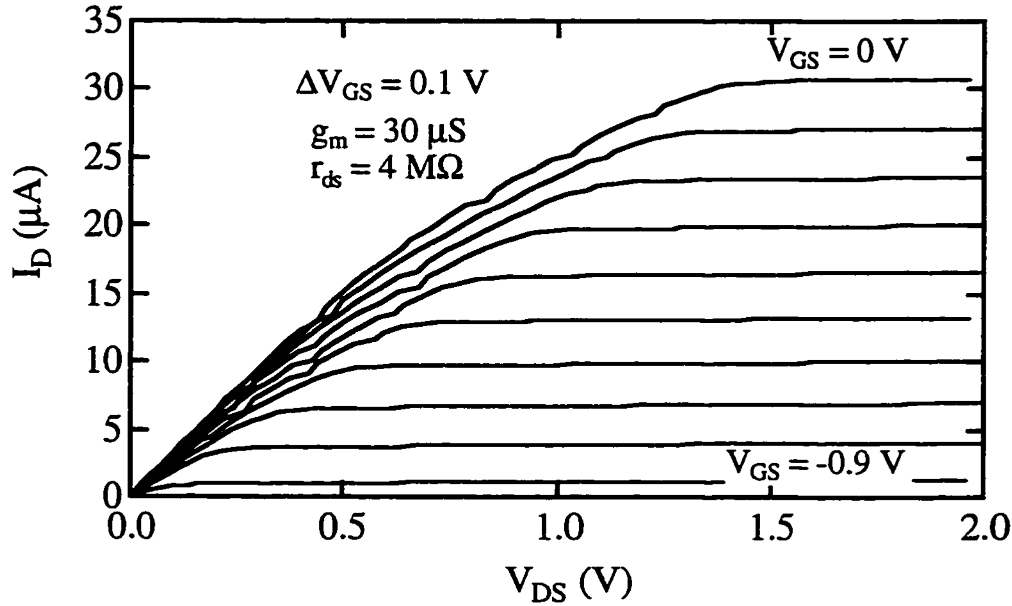


Figure 5.15 Drain-source characteristics I_{DS} vs. V_{DS} of the on-cantilever FET at T = 4.2 K. The gate-source voltage step between drain characteristics is ΔV_{GS} = 0.1 V.

The on-cantilever and reference field-effect transistors were characterized by mounting the sample in vacuum in an Infrared Labs liquid helium Dewar where it was thermally anchored to the cold plate of the Dewar. Low-noise voltage sources were used for the gate-source and drain-source voltages while drain current was monitored using an Ithaco 1211 current amplifier.

Figure 5.15 shows the drain-source characteristics of the on-cantilever field-effect transistor. The small slope of the drain current before saturation is caused by the large, on chip source and drain access resistance $r_{source} + r_{drain} \sim 34$ kΩ. The FET exhibits a typical small-signal drain-source resistance $r_{ds} = 4$ MΩ, and a measured transconductance $g_{mm} = 30$ μS for a drain current $I_D = 10$ μA giving a meaured transconductance per unit gate width of 30 mS/mm. The actual transconductance of the device is larger than the measured value due to the relatively large source access resistance ~ 15 kΩ. The measured tranconductance is defined as $g_{mm} = i_d/v_{gg}$ where i_d is the change in drain current

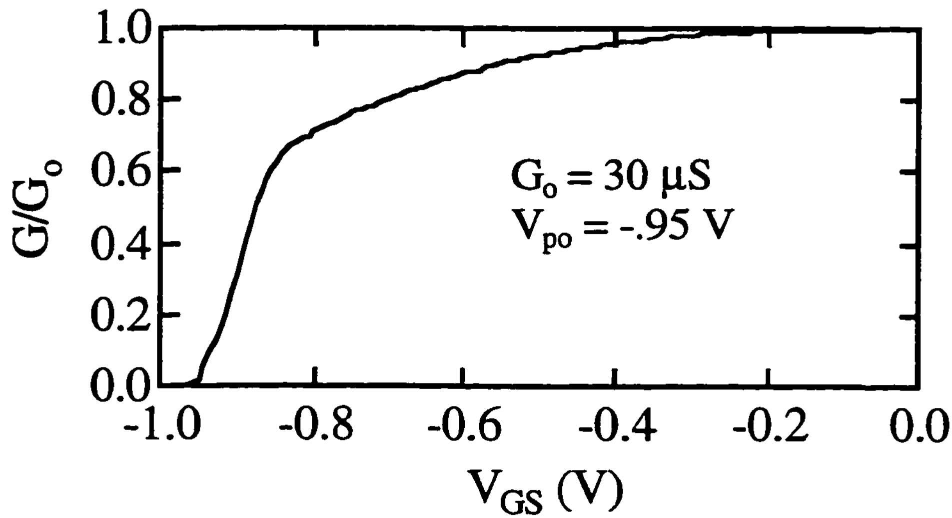


Figure 5.16 Cutoff graph of conductance G normalized to its zero gate-source voltage value G_o = 30 µS for the on-cantilever FET. Conductance decreases as the gate-source voltage is made more negative down to the pinch-off voltage V_{po} = –0.95 F.

and v_{gg} is the change in gate voltage with respect to ground. The actual tranconductance is $g_m = i_d/v_{gs}$ where v_{gs} is the small-signal gate-source voltage. These two are related by

$$g_m = \frac{g_{mm}}{1 - r_s g_{mm}}. \tag{5.8}$$

Thus, for the appreciable source resistance of this device, (possibly ~15 kΩ) the intrinsic device transonductance will be higher than the measured value.

Figure 5.16 shows a graph of channel conductance G normalized to its zero gate voltage value of G_o = 27 µS vs. gate-source voltage V_{GS}. The channel conductance changed by 3 orders of magnitude as the gate voltage approached its pinch-off value V_{po} = –0.95 V.

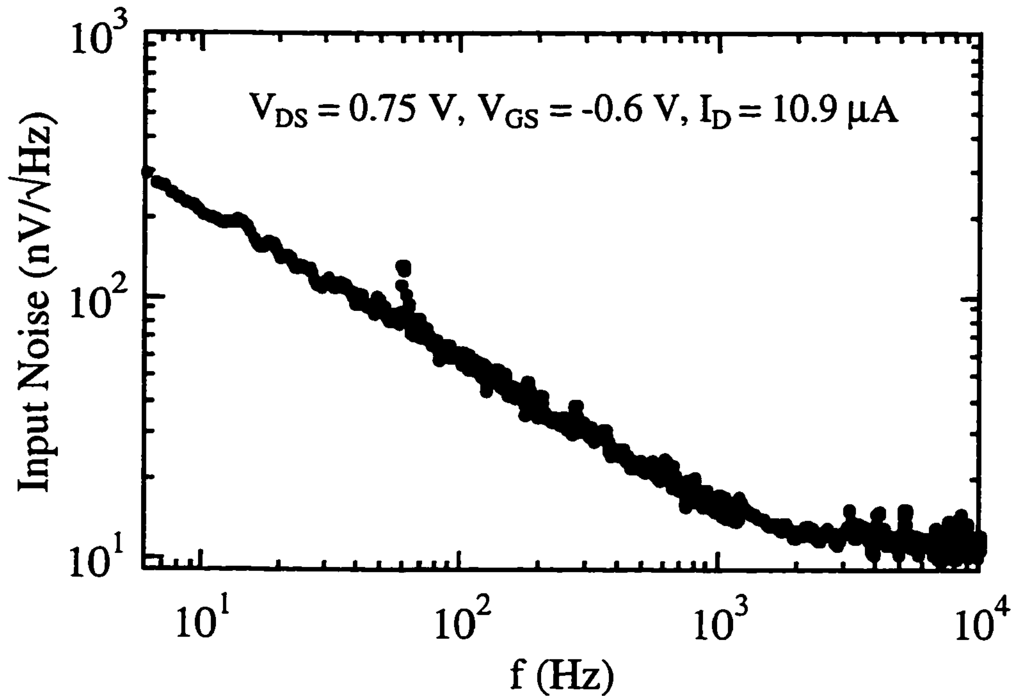


Figure 5.17 Graph of input noise in nV/√Hz for 3μm on-cantilever FET taken at T = 4.2 K. The white noise level is noise due to the external amplifier and corresponds to a gate charge noise of 0.001 e/√Hz.

The measured transconductance was found to be independent of frequency up to 100 kHz, limited by the external circuit. A figure of merit for the intrinsic speed of the transistor is given by $g_m/2\pi C_G$ gives a cutoff frequency of 300 MHz using the measured value of transconductance. Higher cuttoff frequencies could be achieved for devices with smaller source resistance or transistors with shorter and wider channels.

Figure 5.17 shows a voltage noise spectrum for the on-cantilever field-effect transistor. The noise power is characterized by a *1/f* spectrum at low frequencies and is dominated by the white noise level of the Ithaco current amplifier at 2 kHz. The measured current and voltage noise of the Ithaco is 1.3 x 10^{-14} A/√Hz and 23 nV/√Hz on the 10^{-8}A/V scale. This white noise level corresponds to an input voltage noise for the FET gate of about 10 nV/√Hz. This provides an upper bound for the FET gate voltage

noise $\delta v_g = 10$ nV/$\sqrt{\text{Hz}}$ corresponding to a gate charge noise $\delta q_n = 0.001$ e/$\sqrt{\text{Hz}}$. The noise produced by the Johnson noise of the estimated gate metallization resistance and the source access resistace ~ 15 kΩ corresponds to a gate voltage noise ~ 2 nV/$\sqrt{\text{Hz}}$.

5.3.3 Advantages of small cantilevers

The field-effect transistor described above is integrated into a cantilever with dimensions 3 µm x 2 µm x 0.129 µm. This cantilever has a calculated spring constant k = 4.7 N/m and a resonant frequency $f_{res} = 11$ MHz. Below I will list how this device realizes some advantages found in self-sensing cantilevers with integrated FETs.

Because the first stage of the charge amplifier is integrated directly into the region where the charge is produced, charge senstivities are very good. The small cantilever provides a good example of this advantage. The voltage noise level is measured to be less than 10 nV/$\sqrt{\text{Hz}}$ and the gate to channel capacitance is roughly 16 fF implying that the charge noise on the gate is less than 0.001 e/$\sqrt{\text{Hz}}$. This number approaches the sensitivities found with single electron transistors. Because the charge signal is produced directly in the channel region of the FET, it is not capacitivly divided by leads or interconnects. Thus, the FET becomes sensitive to the entire piezoelectrically induced charge.

Another advantage realized as the cantilever becomes smaller is an improved sensitivity to force and displacement. If we assume that the 2DEG screens the charge induced in the well and the two cladding interfaces, then we can write the charge signal $q\Delta n_s$ for a given displacment Δz of the cantilever end or for a given force ΔF applied to the end

$$q\Delta n_s = \frac{3Erd_{12AlGaAs}}{L^2}\Delta z$$

$$q\Delta n_s = 12d_{12AlGaAs}r\frac{L}{wt^3}\Delta F \qquad (5.9)$$

where the parameters are defined in equation (5.2). These expressions can be used to compare the projected sensitivity of the 3 μm x 2 μm x 0.129 μm lever to the measured sensitivity of the 65 μm x 11 μm x 0.25 μm lever shown in Figure 5.7a. The ratio of the charge signal per unit area for the small cantilever over the large cantilever indicates an improvement for the small lever of a factor of 469 in displacement responsivity and 1.9 in force responsivity. Combining this with the improved voltage noise found with the smaller cantilever, $\delta v_{nsmall}/\delta v_{nlarge} \sim 0.1$, we calculate an improvement in displacement sensitivity of about 5000 to $\delta x \sim 0.002$ Å/√Hz and an improvement in force sensitivity of about 19 to $\delta F \sim 1$ pN/√Hz. This demonstrates the improved sensitivity found in smaller cantilevers.

Self-sensing cantilevers can be made thin (thickness ~ 0.1 μm) making possible short cantilevers with high resonant frequency and low spring constants. Because the charge signal depends on the divergence of the polarization, FETs should sense strain even when the quantum well is in the middle of the cantilever. In contrast, piezoresistive cantilevers have a lower limit to their thickness of ~0.25 μm due to the need to confine the diffused piezoresistor to one half of the cantilever for maximum sensitivity. Because GaAs/AlGaAs cantilevers can be made thinner, cantilevers can be fabricated having both a high resonant frequency (~ 11 MHz) and a low spring constant (~4.7 N/m). This high resonant frequency may allow scanning at faster speeds [Walters et al. (1996)].

Finally, the advantage of this small cantilever with an integrated FET is its low power dissipation. This FET will be able to operate with good sensitivity while dissipating only about 10 μW of power. This magnitude of dissipation makes possible

operation with high sensitivity in low temperature environments such as dilution refrigerators and may allow the fabrication of multiple cantilevers on one chip.

CHAPTER 6

SUMMARY AND CONCLUSIONS

In this thesis we have described the fabrication and operation of small mechanical structures made from $GaAs/Al_{0.3}Ga_{0.7}As$ heterostructures and monitored by integrated strain-sensing field-effect transistors (FETs). We have fabricated strain sensing FETs and measured their strain sensitivity to be $2 \times 10^{-9}/\sqrt{Hz}$ at T = 10 K and $4 \times 10^{-9}\sqrt{Hz}$ at T = 77 K. We developed a fabrication process that enabled us to make micro-mechanical structures from heterostructure materials that contain a two-dimensional electron gas (2DEG). We described the operation of three different cantilevers. The first demonstrated dynamic deflection sensing with the FET. The second was used as a low temperature scanning probe microscope cantilever that had a vertical deflection resolution of 10 Å/$\sqrt{Hz}$ at 100 Hz limited by the 1/f noise of the FET. The third was a small cantilever with dimensions 3 μm x 2 μm x 0.129 μm that realized the advantages found in smaller systems. These include increased sensitivity to force and displacement, high resonant frequency for fast operation, and a low spring constant. This cantilever has a projected displacement sensitivity of 0.002 Å/$\sqrt{Hz}$, a resonant frequency of 11 MHz,

and spring constant of 4.7 N/m. Such a cantilever has the potential to scan at high speeds with good sensitivity and low tip to sample forces.

One shortcoming found in the existing devices is that they are not robust; the sample is eventually destroyed by the oxidation of the exposed AlAs layer. Unlike other oxidation processes, AlAs oxidation is not self-limiting; the high strains formed in the Aluminum oxide layer will allow oxidation to continue until the entire device is destroyed. The self-assembled monolayer coating might slow this process allowing our devices to work. Another way to greatly slow this process, possibly to a time scale of years, is by changing the AlAs layer to $Al_{0.9}Ga_{0.1}As$. Layers of this composition can still be etched by HF with a high selectivity over GaAs but will not degrade nearly as rapidly as AlAs in air. This addition may eliminate the need to passivate the samples with a self-assembled monolayer.

The processes developed in this thesis make possible many experiments involving freestanding structures containing a 2DEG. The first, most obvious, extension of this work is to scan with the small cantilever at high speeds. Such a scan could be accomplished using the low temperature SPM in the lab. To demonstrate faster scanning speeds may also require modifying the SPM to incorporate a shorter scanning tube, which has a higher resonant frequency.

The resonant frequency of the small cantilever is calculated to be 11 MHz. A resonance at this frequency may be difficult to excite with piezoelectric bimorphs that generally have resonance frequencies in the kHz range. It would be a great advantage to have the capability to drive the cantilever with the FET gate. Driving the cantilever at resonance amplifies the driving displacement by Q, which would give reasonable

excitation amplitudes for attainable gate voltages in high Q systems. One could then monitor the response of the mechanical system using the same FET by measuring the out of phase response to the driving signal.

This type of driving system could be applied to structures like the mechanical beams used in experiments by Cleland et al. (1997). In their experiments small semiconductor beams capable of carrying current were placed in an 8 T magnetic field where they could be excited with a Lorentz force and their deflection could be monitored by the induced EMF. One could imagine exciting this beam by applying a voltage to a Schottky gate deposited at one end of the beam while monitoring deflection with a strain sensing FET at the other end. This method may make possible the fabrication, excitation and monitoring of a very thin bridge structures e.g. 100 nm. One could imagine looking at the mechanical response of the bridge and possibly observing effects such as single dislocation motion affecting the spring constant or quantum effects on the amplitude.

When making oscillators, it is desirable to have a high Q. As seen from Chapter 2 the minimum detectable force decreases with increasing Q. One problem with our current FET design is that the presence of the gold gate will significantly reduce the mechanical Q of oscillators. One could imagine improving the Q of mechanical structures by making an in-plane gate FET where the gate is defined by an etch trench. The 2DEG on one side of the trench would act as the channel while the gas on the other side would be the gate. Changing the potential of the gate will modulate the 2DEG density in the channel. This configuration may produce devices with working strain sensing FETs and high mechanical Qs.

Strain sensing field-effect transistors are sensitive to the strain induced volume bound charge in the cantilever structure. One could imagine building other types of electronic components that operate using the same effect. One particularly attractive system because of its simplicity and possible high sensitivity is the strain sensing Schottky diode. In this configuration one would have an epitaxial layer of n-type GaAs grown on top of a sacrificial layer. A Schottky gate would be deposited over a strained region of the suspended structure. The forward-biased diode current should have an exponential dependence on induced charge [Sze, (1981)] leading to higher gain. This system should operate at very high speeds and may have increased strain sensitivity.

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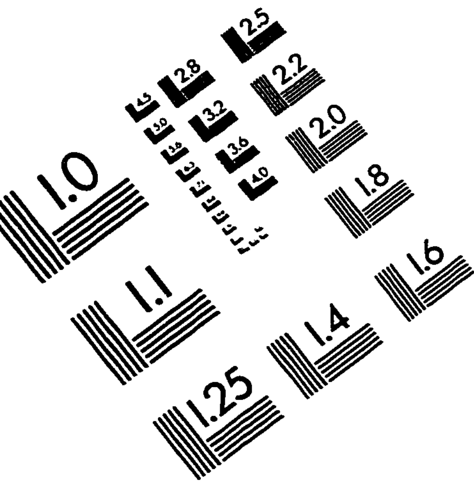
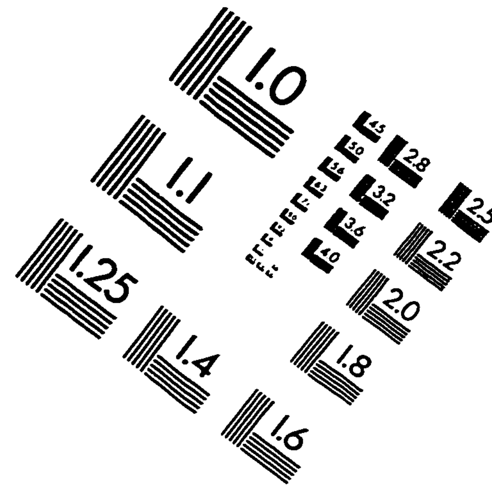
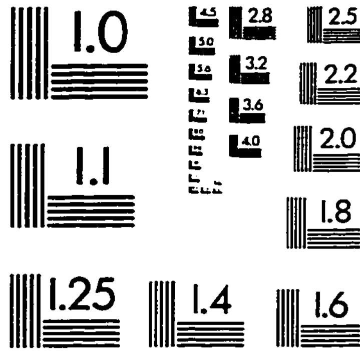
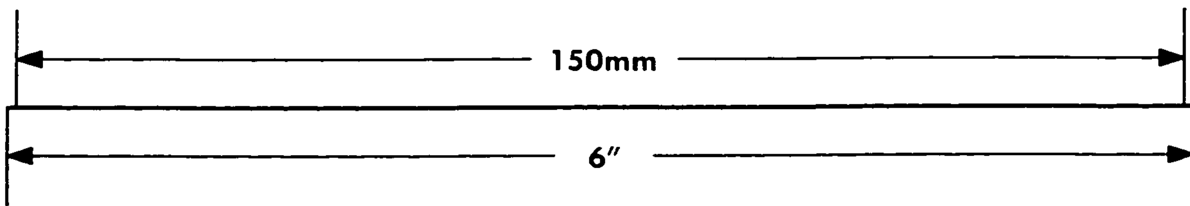
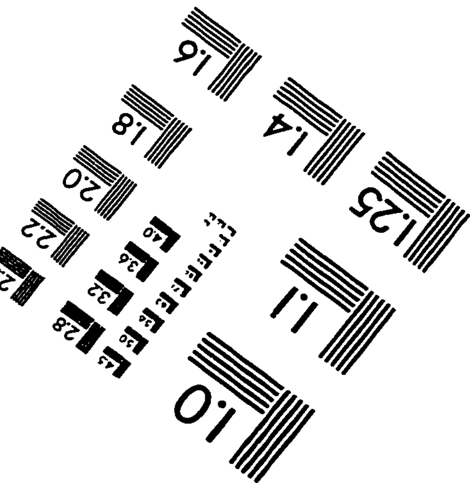
IMAGE EVALUATION TEST TARGET (QA-3)











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